UNIT-1

Ques. What do you mean by doping? Describe its need. Differentiate between N-Type & P-Type semiconductor.

Soln: Doping is the process of adding impurities to intrinsic semi. Trivalent & Pentavalent atoms are used for doping. When trivalent impurities are added then it becomes p-type semiconductor. When penta valent impurities is added then it becomes n-Type semiconductor.

Need of Doping: Doping is done to increase the conductivity of semi conductor devices. Doping creates extra holes or extra electrons to increase the flow of currents. So conductivity of intrinsic semiconductor increases.

DIFFERENTIATE BETWEEN N-TYPE & P-TYPE SEMICOND

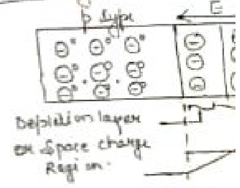
N-Type	P-Type
1. Penta valent impurities such as P, As, Sb are added.	1. Trivalent impurities such as Al, B, Ga are added.
2. Impurities are called donor atom.	2. Impurities are called Acceptor atoms.
3. Majority carriers are electron & minority carriers are holes.	3. Majority carriers are holes & minority carriers are electrons.
4. The donor energy level is close to Conduction Band.	4. The Acceptor energy level is close to Valence Band.

Ques 2. Discuss the formation of depletion layer in diode. Also Explain the effect of temperature on diode.

Soln: When a p-n junction is formed then hole starts to move from p to n & electron starts to move from n to p due to concentration gradient. This is called Diffusion Process. An electric field is gen

---

at the junction, which stops the furt
i.e. a layer of immobile ions is form
called depletion layer or SPACE



Effect of temperature on the P-n

Forward Bias Condition: In this ca
shift to the left at a rate of 2.5
versa.

Reverse Bias Condition:

(a) Reverse Current - Reverse curre
& vice versa. Let I_{S_1} : R
I_{S_2} : R

$$I_{S_2} = I_{S_1} [2$$

Generally it doubles for e

(b) Breakdown voltage (V_Z) - Br
increase in temperature &

Ques 10. Define the term
· What is the value of ripp
Full Wave Rectifier?

ibe its need. Differentiate

puities to intrinsic semicondu
er doping. When it rivalent
pe semiconductors. When Penta
n- type semiconductor.

e the conductivity of semi
or extra electrons to increas
insic semiconductor increases.

& P- TYPE SEMICONDUCTOR

P- Type

ent Impurities such as
Ga are added.

ities are called Acceptor

y carriers are holes &
riers are electrons.

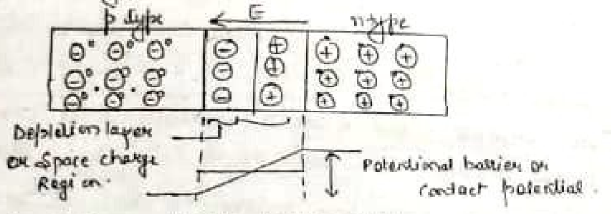
eptor energy level is
lence Band.

in diode. Also

oles starts to move
p due to concentration
lectric field is generated

---

at the junction, which stops the further movement of electrons & holes. So, a layer of immobile ions is formed at the junction. This layer is called depletion layer or SPACE CHARGE REGION



Effect of temperature on the P-n junction diode-

1. Forward Bias Condition: In this case, the characteristics of Si diode shift to the left at a rate of 2.5mv/°c rise in temperature & vice versa.

2. Reverse Bias Condition:

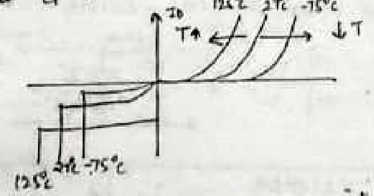
ⓐ Reverse current - Reverse current increase with increase in temperature & vice versa. Let Is_1 : Reverse current at temp. T_1

Is_2 : Reverse current at temp. T_2

$$\boxed{Is_2 = Is_1 \left[2^{T_2 - T_1/10} \right] = Is_1 (2^{\Delta T/10})}$$

Generally it doubles for every 10°c rise in temperature.

ⓑ Breakdown voltage (V_Z) - Breakdown voltage increases with increase in temperature & vice versa.



Ques 10. Define the term Ripple factor. Derive its expression. What is the value of ripple factor for a Half wave Rectifier & a Full wave Rectifier?

Soln: The output of rectifier has AC component (ripple) & dc component both. Ripple factor measure, how much amount of ac component is present in the output. So the effectiveness of a rectifier depends on the magnitude of ripple in the output. Smaller the ripple more effective is the rectifier. "Ripple factor is defined as the ratio of rms value of ac component to the dc component in the rectifier"

$$\gamma = \frac{Iac}{Idc} \quad , \text{but} \quad Iac = \sqrt{Irms^2 - Idc}$$

dividing both sides with Idc

$$\boxed{\frac{Iac}{Idc} = \frac{1}{Idc}\sqrt{Irms^2 - Idc} = \sqrt{\frac{Irms^2}{Idc} - 1}}$$

for Half Wave rectifier : Irms = Im/2 . Idc = Im/π

$$\gamma = \sqrt{\left(\frac{Im/2}{Im/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{4} - 1}$$

$$\boxed{\gamma = 1.21}$$

So ripple factor of Halfwave rectifier is Very High.

for Full wave rectifier [Centre-Tapped Rectifier or Bridge Rectifier]

$$\gamma = \sqrt{\frac{Irms^2}{Idc^2} - 1} \qquad : Irms = Im/\sqrt{2}$$

$$Idc = 2Im/\pi$$

$$\gamma = \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1}$$

$$\gamma = \sqrt{\frac{\pi^2}{4(2)} - 1} = 0.48 \qquad \boxed{\gamma = 0.48}$$

Ques 12. In the bridge rectifier circuit, the secondary voltage $V_s = 100 \sin 50 t$ & load resistance is 1KΩ: (i) DC current (ii) RMS value of current (iii) Efficiency (iv) Ripple factor.

Solⁿ: Given: $V_s = 100 \sin 50t$, $R_L = 1K\Omega$, $r_f = 0$

$V_m = 100$

$$I_m = \frac{V_m}{R_L + r_f} = \frac{100}{1 \times 10^3 + 0} = 100mA$$

$$I_{dc} = \frac{2 I_m}{\pi} = \frac{2 \times 100}{\pi} \times 10^{-3} = 63.66 mA$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{100}{\sqrt{2}} \times 10^{-3} = 70.7106 mA$$

$$\text{Efficiency} = \frac{\text{dc o/p power}}{\text{ac o/p power}}$$

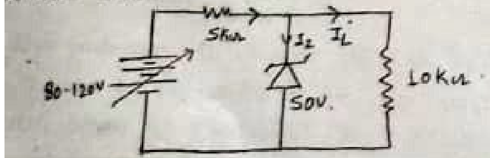
$$\text{dc o/p power} = I_{dc}^2 \times R_L = \left(\frac{200}{\pi}\right)^2 \times 10^{-6} \times 1 \times 10^3$$
$$= 4.0528 W$$

$$\text{ac o/p power} = I_{rms}^2 (R_L + r_f)^0$$
$$= \left(\frac{100}{\sqrt{2}}\right)^2 (1 \times 10^3) = 5.0W$$

$$\text{Efficiency} = \frac{4.052}{5.0} \times 100 = 0.8104 \times 100 = 81.04\%.$$

$$\text{Ripple factor } \gamma = \sqrt{\frac{I_{rms}^2}{I_{dc}^2} - 1} = \sqrt{\left(\frac{70.7106}{63.66}\right)^2 - 1}$$
$$= \sqrt{0.2337}$$
$$\boxed{\gamma = 0.48}$$

us 13. For the circuit shown below, determine the value of aximum & minimum Zener diode current.



Solⁿ: Zener diode acts as the voltage regulator in the circuit & the voltage supply is variable hence, excess of voltage over 50V will across 5kΩ resistance.

Thus, minimum voltage across 5kΩ resistance is 80V-50V

current through 5kΩ resistance is $I_1 = \frac{30}{5000} = 6mA$

Also, maximum voltage across 5kΩ resistance is 120V-50V=7

current through 5kΩ resistance is $I_1' = \frac{70}{5000} = 14mA$

Now, voltage across load resistance of 10kΩ is 50V

Thus, current through 10kΩ will be $I_2 = \frac{50}{10000} = 5m$

Hence, maximum current through Zener diode is

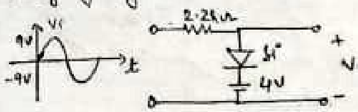
$$I_Z = I_1' - I_2 = 14 - 5 = 9mA$$

minimum current through zener diode is

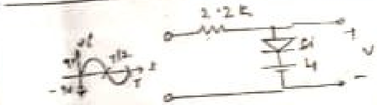
$$I_Z = I_1 - I_2 = 6 - 5 = 1mA$$

$$\boxed{I_{Z\,max} = 9mA}$$
$$\boxed{I_{Z\,min} = 1mA}$$

Ques 14 Differentiate between clipper & clamper circuit. Determ draw output voltage for given network.



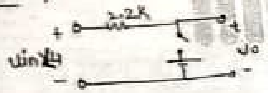
CLIPPER	CLAMPER
1. Clipper delimit the amplitude of the output voltage.	1. Clamper shifts the DC level of the output voltage.
2. Output voltage is less than the input voltage.	2. Output voltage is multiples of i voltage.
3. Energy storage component is not required.	3. Energy storage component is requi i.e Capacitor is used.
DC level remains same.	4. DC leve
5. Shape of the output waveform changes.	5. Shape of remains sa
Applications : Transmitters, Recievers, amplitude selector etc.	6. Applicatio circuits, S



Case 1 0 to T/2 ; when vin>4V ,

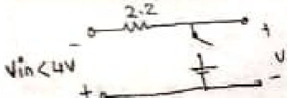
$\boxed{V_0 =}$

vin<4V , Diode is Reverse Bias , hence

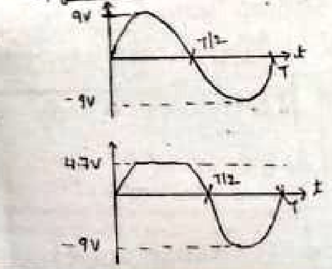


$\boxed{V_0 = v_{in}}$

Case 2 T/2 to T ; when vin<4V ,



$\boxed{V_0 =}$



or in the circuit & the
voltage over 50V will be

sistance is 80V - 50V = 30

$\frac{30}{000}$ = 6mA

is 120V - 50V = 70V

$\frac{}{00}$ = 14mA

is 50V

2 = $\frac{50}{10000}$ = 5mA

le is

2 = 14 - 5 = 9mA

is

= 6 - 5 = 1mA

circuit Determin

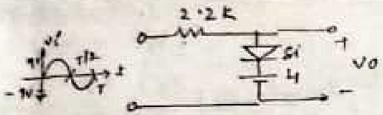
PER

DC level of the

multiples of input

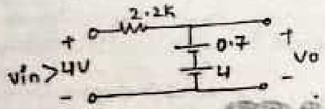
onent is required

4. DC level remains same.	4. DC level get shifted.
5. Shape of the Output waveform changes.	5. Shape of the Output waveform remains same as input waveform.
6. Applications : Transmitters, recievers, amplitude selector etc.	6. Applications : In Voltage multiplier circuits, Sonar, Radar system etc.



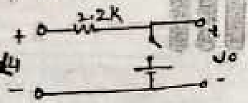
Shunt Clipper -

Case1 0 to T/2 ; when vin>4V , Diode is forward Bias as for Si V_γ = 0.7V



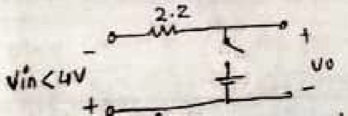
$\boxed{V_0 = 0.7+4 = 4.7V}$

vin < 4V , Diode is Reverse Bias , hence open switch.

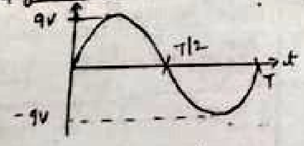


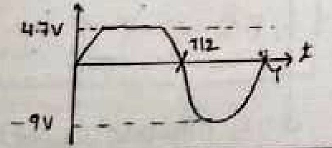
$\boxed{V_0 = V_{in}}$

Case2 T/2 to T ; when vin < 4V , Diode will be Reverse Bias, hence open switch

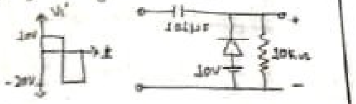


$\boxed{V_0 = V_{in}}$



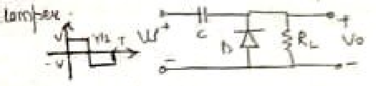


Ques15 Explain Positive & Negative clamper using suitable circuit diagram & input/output waveform. Determine output voltage for the given network.



Soln: **Positive Clamper :**

It shifts the ac signal in upward direction then clamper is called positive clamper.

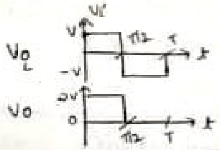


Case1: 0 to T/2 ; Diode is Reverse Bias
Capacitor is charged to -Vi

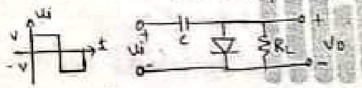
$\boxed{V_0 = 2V}$

Case2: T/2 to T ; Diode is Forward Bias
capacitor is charged

$\boxed{V_0 = 0}$



Negative clamper : It shifts the ac signal in downward direction. then clamper is called Negative clamper.

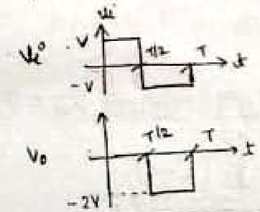


Case1: 0 to T/2 ; Diode is Forward Bias. Capacitor is charged to Vi

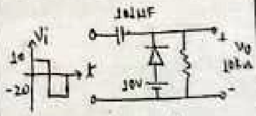
$\boxed{V_0 = 0}$

Case2: T/2 to T ; Diode is Reverse Bias
Capacitor is charged.

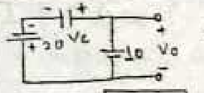
$\boxed{V_0 = -2V}$



Positive Clamper :



Negative Cycle : Vin = -20
Diode is ON & circuit is drawn.

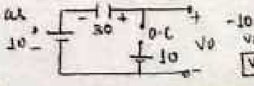


+20 - Vc + 10 = 0

$\boxed{V_c = 30}$

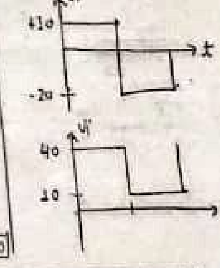
$\boxed{V_0 = 10V}$

Positive cycle :- Vin = 10
Diode is OFF & circuit is drawn as



-10 - 30 + Vo = 0

$\boxed{V_0 = 40}$



(Q.3) Draw & explain the V-I characteristic of a P-N Junction diode. Also describe the effect of temperature on diode.

Sol: <u>V-I characteristic of P-N Junction diode :-</u>

diode current equation is:-

$$I_D = I_S [e^{V_D/\eta V_T} - 1] \quad \text{—①}$$

where I_D = diode current

I_S = Reverse saturation current

V_D = diode voltage

V_T = volt equivalent of temperature

η = Ideality factor for $\eta = 1 \rightarrow$ Ge

Si $\rightarrow \eta = 2$

$V_T = \frac{T}{11600}$ volt (T should be in kelvin) at room temp $V_T = 26$ mV.

① Unbiased condition:- $V_D = 0$

$$I_D = I_S [e^{V_D/\eta V_T} - 1] \quad \text{where } V_D = 0$$

then

$$I_D = I_S [e^{0/\eta V_T} - 1] = I_S [1 - 1]$$

$$I_D = I_S [0] = 0 \quad \boxed{I_D = 0}$$

So curve passes through the origin.

⑪ Forward bias condition:- $V_D = +ve$

$$I_D = I_S [e^{+V_D/\eta V_T} - 1]$$

But $e^{V_D/nV_T} >>> 1$

Therefore equation 1 becomes

$$I_D \simeq I_S (e^{V_D/nV_T})$$

Hence forward characteristics is of exponential in nature

(iii) <u>Reverse bias:-</u>

$$V_D = -ve$$

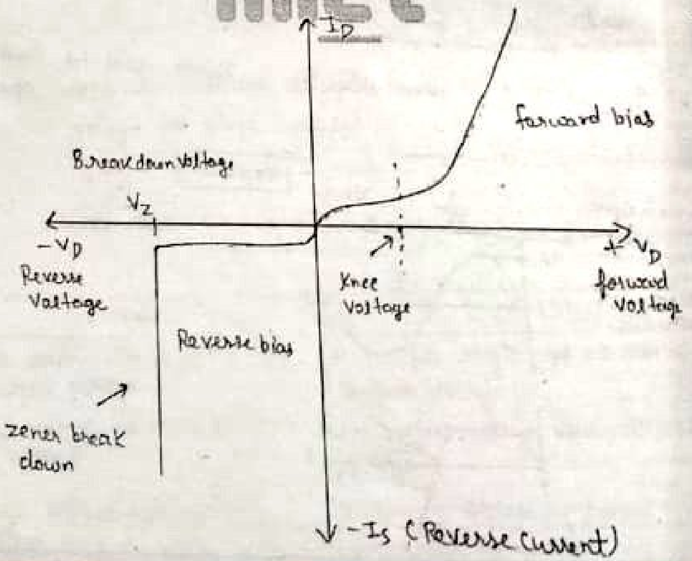
$$I_D = I_S [e^{-V_D/nV_T} - 1]$$

$$= I_S [\frac{1}{e^{V_D/nV_T}} - 1]$$

But $\frac{1}{e^{V_D/nV_T}} <<< 1$

So equation 1 becomes

$$I_D \cong -I_S$$



effect of temperature o

ⓐ Forward bias:- In case

of si diode shift to the

temp. and vice-versa.

ⓑ Reverse bias Condition:- (

with increase in temp. a

at temp T_1 then at temp

$I_{S_2} = I_{S_1} [2^{T_2 - T}$

$\boxed{I_{S2} = I}$

① Breakdown voltage (V_Z):- Breakd

Q.4 (i) explain the knee

the Reverse sa

is 10 µA at 300k. d

applied to obtain d

Sol: knee voltage:

required to start

this minimum

or cut-off

for Ge

for Si

effect of temperature on V-I characteristic of PN Junction diode:-

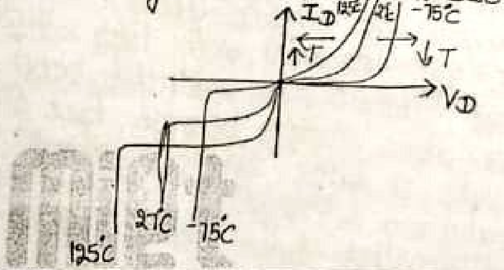
ⓐ **forward bias:-** In case of forward bias region the characteristic of si diode shift to the left at a rate of 2.5 mV/°C rise in temp. and vice-versa.

ⓑ **Reverse bias Condition:-** ① **Reverse current:-** Reverse current increase with increase in temp. and vice versa. Let I_{S1} is the reverse current at temp T_1 then at temp T_2. I_{S2} can be calculated as:-

$$I_{S2} = I_{S1}\left[2^{T_2-T_1/10}\right] = I_{S1}\left[2^{\Delta T/10}\right]$$

$$\boxed{I_{S2} = I_{S1}\left[2^{\frac{\Delta T}{10}}\right]}$$

⑪ **Breakdown voltage (Vz):-** Breakdown voltage increases with increase in temp



Q.4 ① Explain the knee voltage. what is knee voltage of Ge, Si p ② the Reverse saturation current of Si Pn Junction diode is 10 μA at 300k. determine the forward bias voltage to be applied to obtain diode current of 100 mA.

Sol: **knee voltage:-** A minimum positive voltage is required to start conduction in a forward biased diode. this minimum positive voltage is called knee voltage or cut-off voltage (V_γ).

for Ge	$V_\gamma = 0.3V$
for Si	$V_\gamma = 0.7V$

Q.4 The reverse saturation current of Si P-n junction diode is 10μA at 300K. Determine the forward bias voltage to be applied to obtain diode current of 100mA.

Ans

$$I_D = I_s[e^{V_D/nV_T} - 1]$$

$$100\times10^{-3} = 10\times10^{-6}\left[e^{V_D/2\times0.026} - 1\right]$$

$$10001 = e^{V_D/0.0518}$$

taking ln on both side

$$9.21 = \frac{V_D}{0.0518}$$

$$V_D = 0.47V$$

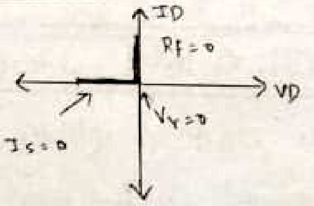
Q.5. Explain the V-I characteristics of ideal diode in Forward bias & Reverse bias Conditions. Give all the equivalent / approximation circuits of a diode.

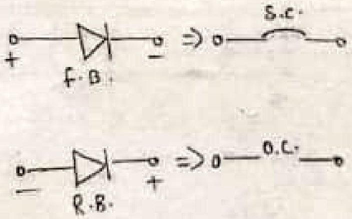
Ans **Ideal equivalent circuit**

In ideal diode, $R_f = 0$, $V_\gamma = 0$ and $I_s = 0$.

An ideal diode can be used as a perfect switch.

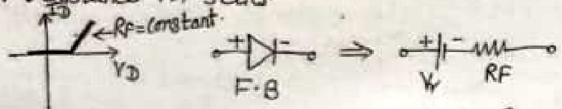
V-I characteristics-



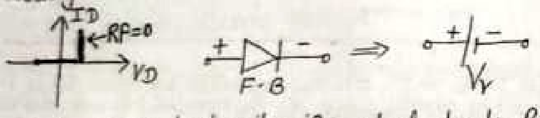


Equivalent circuits of a diode :-

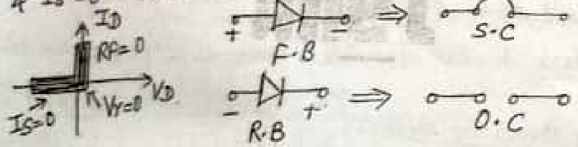
① Piecewise Linear equivalent circuits :- In this circuit diode can non linear characteristics is replaced by a straight line. So resistance of diode is constant. diode is replaced by battery with resistance in series.



(ii) Simplified equivalent circuits :- Since diode forward resistance is Low. So It can be neglected i.e RF=0 diode is replaced by battery.



(iii) Ideal equivalent circuit :- In ideal diode RF=0, Vr=0 & Is=0 An Ideal diode can be used as a Perfect switch



(Q.6) describe breakdown mechanism of diode.
differentiate between avalanche and Zener breakd

Sol: breakdown Mechanism :- If the reverse bias of
to P-N Junction is increased, a point will reach
the Junction breakdown & reverse current rises sharply
this specific value of the reverse bias voltage is call
breakdown voltage (V_z). the following two process cause Jun
breakdown. ① Zener breakdown :- It occurs in highly
doped diode. In highly doped diode width of depletion
is narrow. So electric field is very high. in deplet
Layer. So Force is very high. this high force pull
Valance electron into conduction band by breaking cov
bonds. these electrons become free electrons and will
constitute a large reverse current. this is called Zener
breakdown is negative i.e raising the temp. will
cause smaller break down voltage.

② Avalanche Breakdown :- It occurs in lightly dope
diode. In lightly doped diode width of depletion
is wide. So electric field and force are low.
this Low Force can not break the covalent bo

As reverse voltage is increased the kin
energy ($\frac{1}{2}mv^2$) of minority carriers increase
while travelling these minority carriers will
colloide with the stationary atom present in d
Layer & impart some of the kinetic en
to the valance electrons. these valance el
will break their covalent bond and Jump
conduction band to become Free electrons.

Differentiate between avalanche
breakdown.

S.N.	Zener Breakdown	A
1.	Occurs in highly doped diode	occ diod
2.	The valence electrons are pulled into conduction band due to very high electric field	The are band im of ca
3.	Tunneling effect occurs	Io occ
	Occurs less than 6v	occ
5.	Zener breakdown V-I characteristics is very sharp.	It i tha
6.	Covalent bonds breaks directly.	Cov ind
7.	Temperature coefficient is negative.	Te is

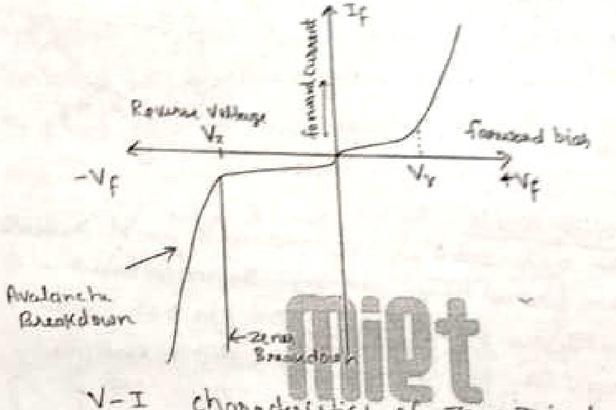
af diode.
d Zener breakdown
reverse bias applie
t will reach when
rises sharply.
oltage is called
ces cause Junction
curs in highly
af depletion lay
b. in depletion
force pulled b
eaking covalent
and will
called Zener
temp. will

ghtly doped
depletion regi
e low.
valent bond.
the kineti
ncreases
will
in deplet
c energy
e electr
mp into
ns.

Differentiate between avalanche and zener breakdown.

S.N.	Zener Breakdown	Avalanche Breakdown
1.	Occurs in highly doped diode	Occurs in lightly doped diode.
2.	The valence electrons are pulled into conduction band due to very high electric field	The valence electrons are pushed into conduction band due to the energy imparted by collision of accelerated minority carrier.
3.	Tunneling effect occurs	Ionization effect occurs.
4.	Occurs less than 6v	Occurs greater than 6v.
5.	Zener breakdown V-I characteristics is very sharp.	It is not as sharp as that zener diode
6.	Covalent bonds breaks directly.	Covalent bonds break indirectly.
7.	Temperature coefficient is negative.	Temperature coefficient is positive.

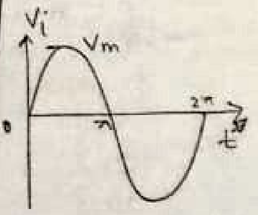
Zener Diode Symbol

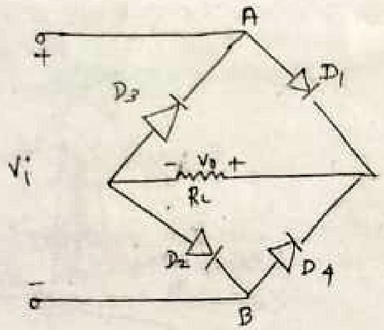


V-I characteristics of Zener Diode

Q.9 Explain the working of Bridge rectifier with diagram and derive the expression for rectification efficiency. what is PIV of Bridge Rectifier?

Ans- The bridge rectifier uses four diodes which are connected in bridge pattan.

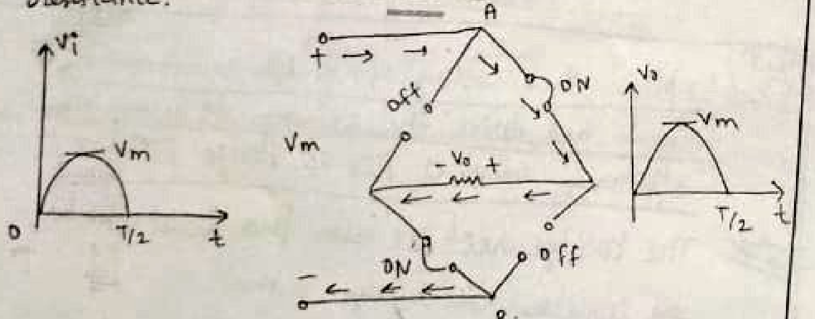




Warking-

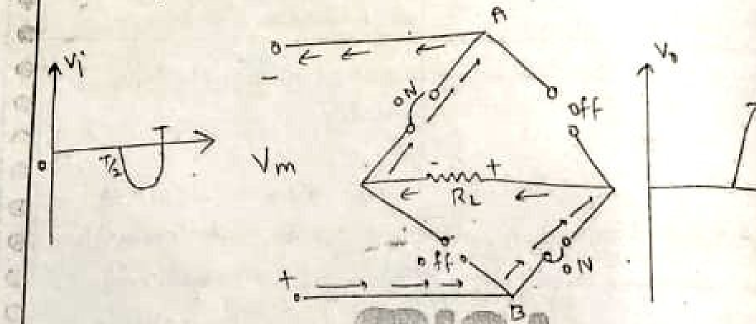
(1) for positive cycle-

In positive cycle end A is +ve and end B is -ve. So diode D1, D2 are forward biased and D3, D4 are reverse biased. So, D1, D2 are ON and D3, D4 are Off. Current flows through D1, D2 and give the output across load resistance.

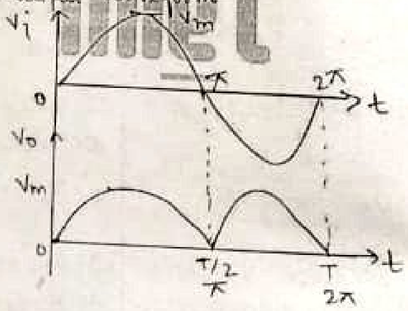


---

ii) for negative cycle- In negative cycle end A is negative and end B is positive. So diodes D1, D2 are reverse biased and D3, D4 are forward biased. So D1, D2 are off and D3, D4 are ON. Current flows through D3, D4 and give the output across load resistance RL.



Input and output waveform



Rectification efficiency:-

$$\eta = \frac{dc\ o/p\ Power}{ac\ I/P\ Power} = \frac{P_{o(dc)}}{P_{i(ac)}}$$

$$= \frac{I^2_{dc} \times R_L}{I^2_{rms} \times (R_L + r_f)}$$

$$= \frac{\left(\frac{2I_m}{\pi}\right)^2 \times R_L}{\left(\frac{I_m}{\sqrt{2}}\right)^2 \times (R_L + r_f)}$$

If $r_f = 0$

η_{ma}

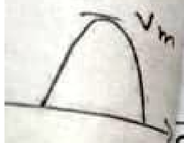
$\boxed{PIV:- V_m}$

= Compare halfwave and

=

N.	Parameter	Half wave rectifier	centre tap Rectifie
	Operation	Conducts during positive half cycles.	Conduct both th cycles
	V_{dc}	$\frac{V_m}{\pi}$	$\frac{2V_m}{\pi}$
	V_{rms}	$\frac{V_m}{2}$	$\frac{V_m}{\sqrt{}}$
	Ripple factor	1.21	0.4
	Efficiency	40.6%	81.2
	PIV	Vm	2V
	Ripple freq.	$f_r = f_i$	$f_r =$

l A is negative
everse biased
are off
h D3, D4



(dc)
(ac)

$$= \frac{\left(\frac{2I_m}{\pi}\right)^2 \times R_L}{\left(\frac{I_m}{\sqrt{2}}\right)^2 \times (R_L + r_f)}$$

$$\eta = \frac{0.812}{1 + \frac{r_f}{R_L}}$$

If $r_f = 0$

$$\eta_{max} = 0.812$$
$$= 81.2\%$$

$\boxed{\text{PIV:- } V_m}$

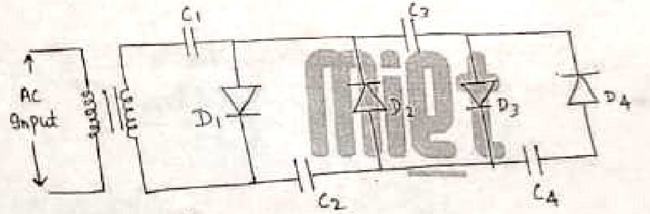
07 Compare halfwave and full wave rectifier.

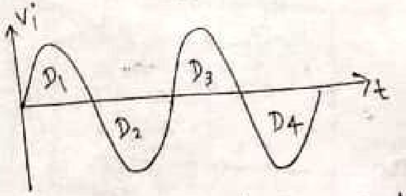
Ans-

S.N.	Parameter	Half wave rectifier	Full wave centre tapped Rectifier	Full wave Bridge Rectifier
1.	Operation	Conducts during positive half cycles.	Conducts during both the half cycles	Conducts during both the half cycles
2.	V_{dc}	$\frac{V_m}{\pi}$	$\frac{2V_m}{\pi}$	$\frac{2V_m}{\pi}$
3	V_{rms}	$\frac{V_m}{2}$	$\frac{V_m}{\sqrt{2}}$	$\frac{V_m}{\sqrt{2}}$
4	Ripple factor	1.21	0.48	0.48
5	Efficiency	40.6%	81.2%	81.2%
6	PIV	V_m	$2V_m$	V_m
7	Ripple freq.	$f_r = f_i$	$f_r = 2f_i$	$f_r = 2f_i$

Q:7 Explain the multiplier circuit (halfwave double, tripler, Quadruple). / Define voltage Multiplier. Draw the circuit & explain working of voltage tripler & Quadrupler circuit

Ans- This circuit diagram is a general voltage multiplier circuit. It can perform function of Voltage doubler, tripler, Quadrupler. So for doubler two diodes and two capacitor are needed for tripler three diodes and three capacitor are needed. If we need nV_m at output we have to use n-diode & n capacitor.





Working:- for the first positive cycle:- D1 is ON. So capacitor C1 charges up to Voltage Vm.

$$V_{C1} = V_m$$

for first negative cycle:- D2 is ON. So capacitor C2 charges up to Voltage 2Vm.

Applying KVL

$V_m + V_{C2} - V_m = 0$

$V_{C2} = 2V_m$

(iii) for second positive cycle :-

D_3 is ON. So capacitor C_3 charges upto Voltage $2V_m$

Applying KVL

$-V_m + 2V_m - V_{C3} + V_m = 0$

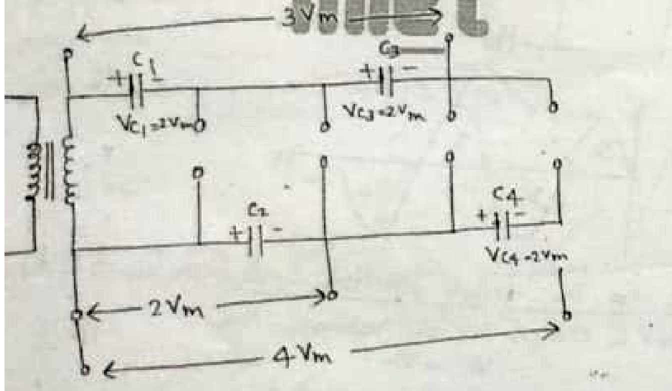
$V_{C3} = 2V_m$

(iv) · for second negative cycle :-

D_4 is ON. So capacitor C_4 charges upto voltage $2V_m$.

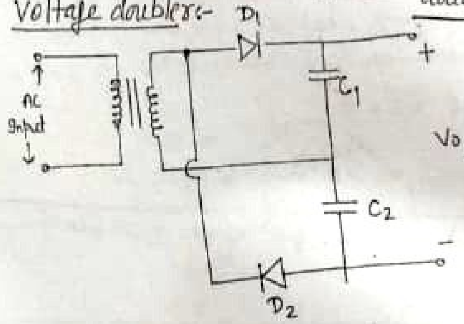
Applying KVL:- $-V_m - 2V_m + V_{C4} + 2V_m - V_m = 0$

$V_{C4} = 2V_m$

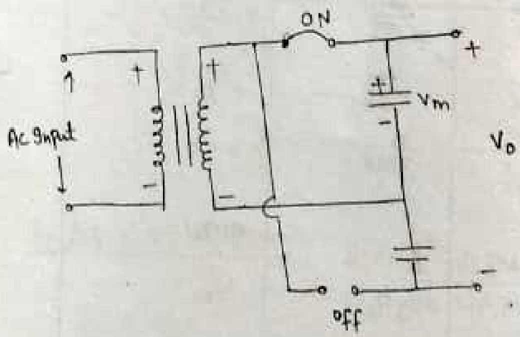


(Q.8) Explain the working of full wave Voltage doubler with help of a neat diagram. (or) explain the working of a voltage doubler circuit.

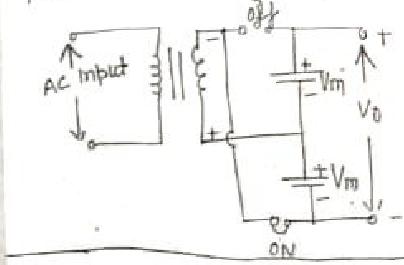
Ans- Voltage doubler:-



Working- (i) for positive cycle- In positive cycle D_1 forward biased but D_2 is reverse biased. So capaci charges upto voltage V_m.



(ii) for negative cycle:- In negative cycle reverse biased but D_2 is forward bi capacitor C_2 charges up to voltage Vm

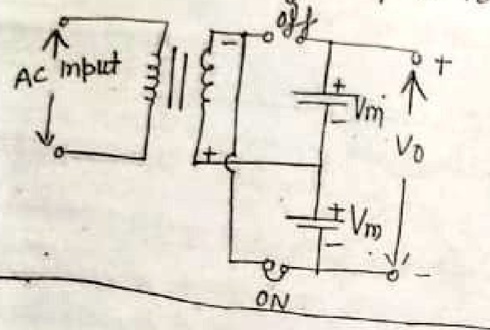


So · Vo=

Vo=

$\boxed{V_0 =}$

(ii) **for negative cycle:-** In negative cycle D1 is reverse biased but D2 is forward biased. so capacitor C2 charges up to voltage Vm.

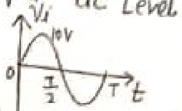


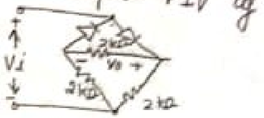
So. $V_o = V_{C1} + V_{C2}$

$V_o = V_m + V_m$

$\boxed{V_o = 2V_m}$

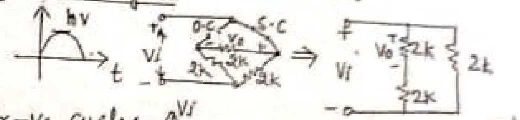
(Q11) why bridge type full wave rectifier is preferred over centre taped full wave Rectifier. state two reason. determine output the waveform for the given N/w below. Also determine the output dc Level and compute PIV of each diode.





$V_o = \frac{1}{2} V_i$ or $\frac{1}{2} V_{imax}$

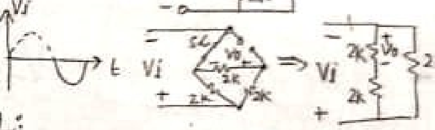
Sol. for +ve cycle



$V_o = \frac{1}{2} \times 10$

$\boxed{V_o = 5V}$

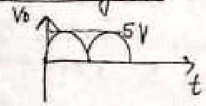
For -ve cycle:-



$V_o = \frac{1}{2} V_i = \frac{1}{2} V_{imax}$

$V_o = \frac{1}{2} \times 10 = 5V$

So o/p wave form:

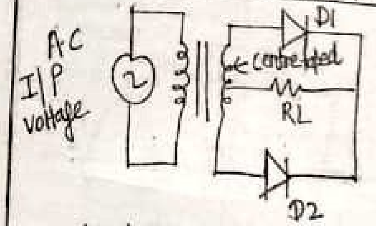


$V_{dc} = \frac{2V_m}{\pi} = 0.636 V_m$

$= 0.636 \times 5 = 3.18$

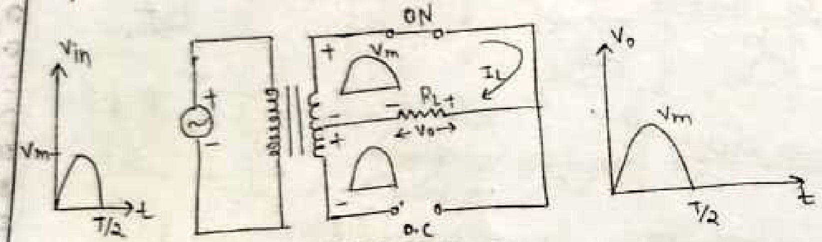
$\boxed{PIV = 5V}$

Centre taped Full wave Rectifier:-

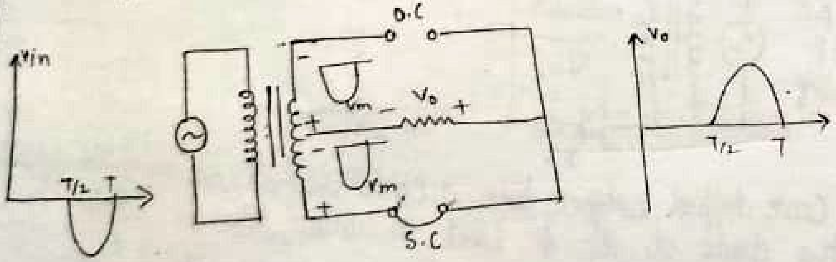


Cente tapped Rectifier have a centre tapped stepdown transformer two diode d1, d2 & Load resistance RL. In centre tapped transformer secondary winding is divided in two equal halfs.

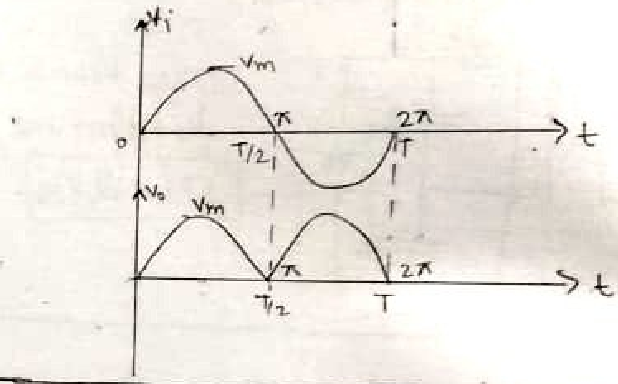
<u>Working</u>- (i) for positive half cycle. In positive half cycle diode D_1 is forward biased and D_2 is reverse biased. So D_1 is ON and D_2 is ~~reverse biased~~ off. Current flows through the upper half of secondary Winding.



(ii) for negative cycle- In negative cycle diode D_1 is reverse biased and diode D_2 is forward biased. So D_1 is off and D_2 is ON. current flows through the lower half of secondary Windings.



<u>Input and output wave of rectifier</u>:-



Q16- Explain Working and characteristic of Tunnel diode & LED with the help of neat diagram

(a) <u>Tunnel Diode</u>

(b) <u>LED</u>

<u>Ans</u>- <u>Tunnel Diode</u>:-

Tunnel diode symbol

- → Tunnel diode is very highly doped diode.
- → The doping of tunnel diode is 1000 times gre than simple diode.
- → So, depletion layer is very narrow and is of the order of 10nm.

---

rking of tunnel

Unbiased tun

of n type over

) Small Voltag

then a sm

tunnel to

i) Applied V

increased.

exactly e

) Applied V

of condu

Applied V

band and

operate w

I

Iv

-V ←

Working of tunnel diode-

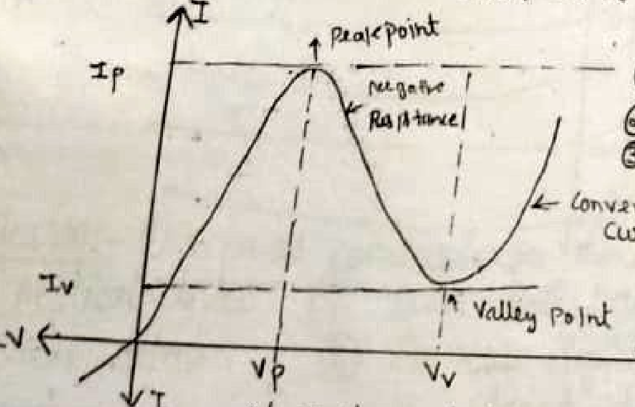
(i) **Unbiased tunnel diode-** Due to high doping the conduction band of n type overlaps with the Valence band of p-type material

(ii) **Small Voltage is applied-** When a small Voltage is applied, then a small number of electrons from conduction band tunnel to the Valence band.

(iii) **Applied Voltage is slightly increased-** When Voltage applied is increased, the energy level of n side conduction band becomes exactly equal to the energy level of p-side Valence band.

(iv) **Applied Voltage is further increased-** A slight misalignment of conduction band and Valence band takes place.

(V) **Applied Voltage is largely increased-** At this point the conduction band and Valence band no longer overlap and tunnel diode operate in the same manner as a normal diode.



V-I Characteristics of tunnel diode

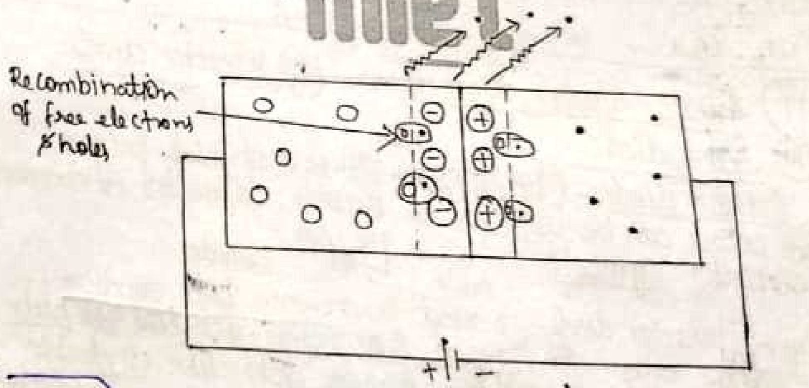
Application:-

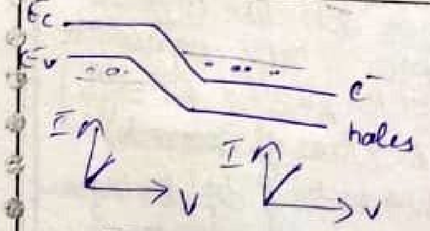
① Used as Logic memory storage device.
② Used in FM Receiver
③ Used as an Ultra high speed switch

ⓑ **LED-** Light Emitting diode (LED) is a photo electronic device Which converts electrical energy into light energy. material like gallium, phosphorus and arsenic are used for the manufactaing of LED.

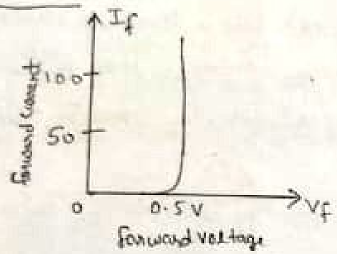
Symbol

Working- When LED is forward biased then hole in p-type and electron in n-type start to cross the junction and recombine with each other. Simple diode (Ge, Si) produce heat in recombination.





V-I characteristics:-



Application:- :-

1) used in digital clocks
2) used in calculators.
3) used in mobile TV displays
4) used in seven segment displays.

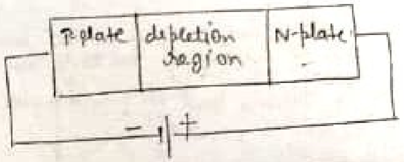
Q.17 Write shortes Note on:- ⓐ Varactor diode
ⓑ Photo diode

Sol: Varactor diode:- (VARICAP):- It is a special purpose diode which can be used as a Variable capacitor in microwave circuit. Symbol:- 

Working:- Varactor diode is used in reverse bias condition. In reverse bias. the P region & N region act like the plate of capacitor. while the depletion region acts like dielectric So there exists a capacitance space charge capacitance or depletion region capacitance. It is given by $\boxed{C_T = \frac{\epsilon A}{W}}$

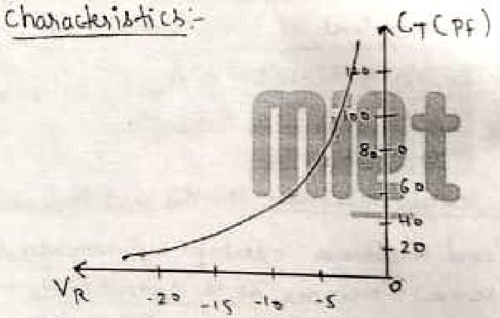
$\epsilon \rightarrow$ permittivity of semiconductor $A \rightarrow$ Area of cross section

$W \rightarrow$ width of depletion region.



→ As the reverse bias applied to the diode increases width of depletion region (W) increases. So C_T decreases and vice-versa. Therefore capacitance controlled by applied Voltage.

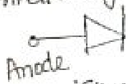
Characteristics:-



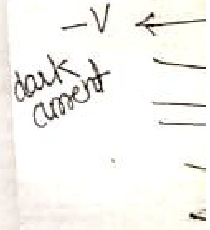
Application-

- Fm modulator
- Tunning circuit
- In TV receiver
- In radio receiver

oto diode:- A phot
ce that converts lig



king:- when a light
d to illuminate p-
ton hits the Immobi
If energy of ph
d will break. So
Due to electric
om the Junction
lectrons moves
urrent. this
electric effe
I characteristi



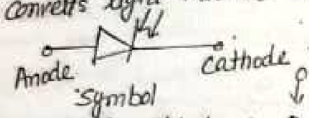
Application:-
③ Medical
④ Smoke

iode increase, the

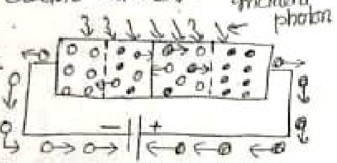
es. So, CT

apacitance can be

Photo diode:- A photo diode is a semiconductor P-N Junction device that converts light into an electric current.



Symbol

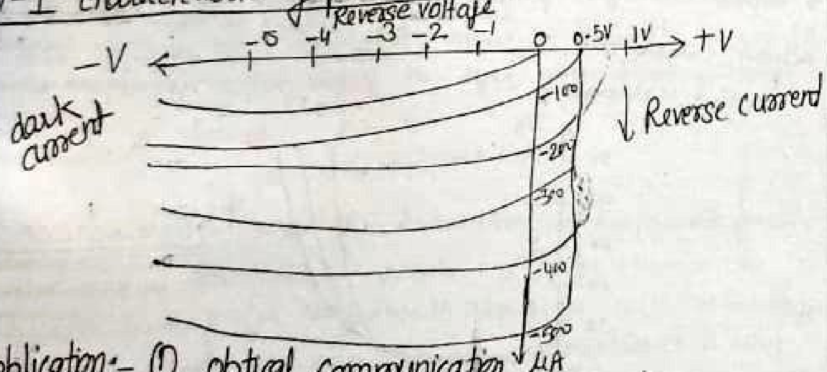


Working:- when a light or photon is used to illuminate p-n Junction than photon hits the Immobile ions present in the depletion layer.

⇒ If energy of photon is greater than 1.1 ev than covalent bond will break. So electron hole pair are generated.

⇒ Due to electric field electron hole pairs move away from the Junction. Hence holes moves to anode & electrons moves to the cathode to produce photo current. this entire process is known as photo-electric effect.

V-I characteristic of photo diode:-



Application:- ① optical communication
② Medical device ③ solar cell pannels
④ Smoke detectors ⑤ Camera light meters and street lights.

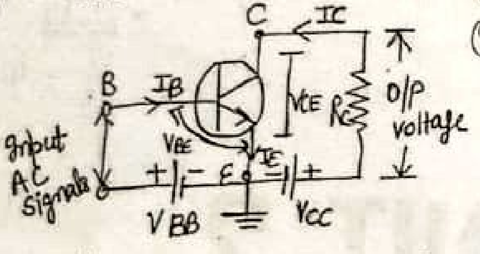
1.1 eV

UNIT-2

UNIT- 2ND

Q.1 Describe the construction and Working of a NPN transistor in CE configuration w.r. to size and doping. Also draw the input output characteristic graph.

Sol: CE (Common Emitter (Configuration)) :- In CE configuration input is applied b/w base and emitter while output is taken out from collector and emitter. So emitter of transistor is common to both input and output.



① DC current gain (β):-

It is the ratio of O/P current (I_C) to the input current (I_B).

$$\boxed{\beta = \frac{I_C}{I_B}}$$

Since value of $I_B << I_C$ so $\beta >> 1$.
So current gain is available in CE Configuration.
Value of β varies from 20 to 500.

⑪ Expression for output current:- $I_C = \alpha I_E + I_{CBO}$

$$I_C = \alpha(I_C + I_B) + I_{CBO} \quad (I_E = I_C + I_B)$$

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

$$I_C = \alpha I_C + \alpha I_B + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO} \quad \text{— ①}$$

but $\beta = \frac{\alpha}{1-\alpha} \Rightarrow \frac{\alpha}{1-\alpha} + 1 = \beta + 1$

$\frac{1}{1-\alpha} = \beta + 1 \quad \frac{1}{1-\alpha} = \beta + 1$ — ② using eq① & eq②

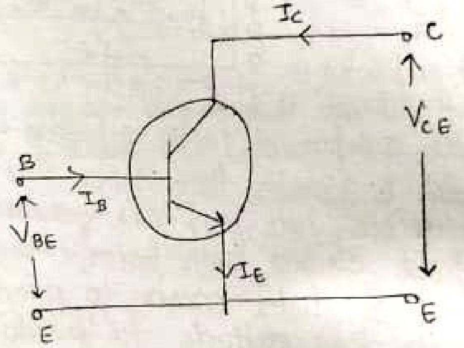
$I_C = \beta I_B + (\beta+1) I_{CBO}$

$\boxed{I_C = \beta I_B + I_{CEO}}$

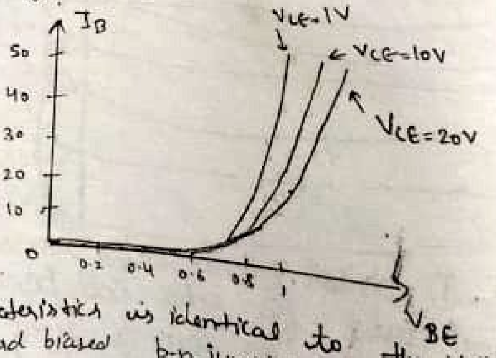
where I_{CEO}: leakage current b/w collector & emitter while base is open i.e $I_B = 0$ $I_{CEO} = (\beta+1) I_{CBO}$

Q-1 Draw the input and output characteristics of common emitter configuration. :-

Ans-



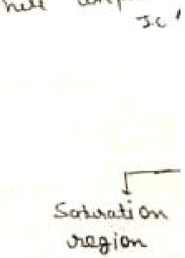
Input Characteristics- It is the graph between input current & input voltage for a constant output voltage. In input current is I_B and input voltage is V_{BE} while output voltage is V_{CB}.



- Input characteristics is identical to the V-I characteristics of forward biased p-n junction diode.

tput characteristics-

Current and output
for CE output
VCE while input

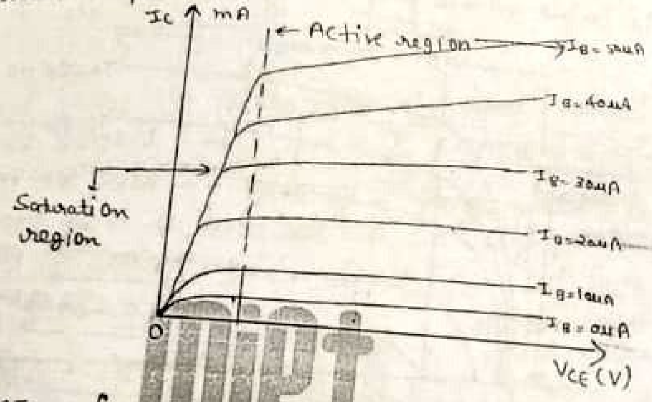


Active Region-
ICBO, which is mo
so graph of ac
in IC on chan

Saturation region-
active region to
Collector curren

cutoff region- When
small collector C
In CE configura

Output characteristics- It is a graph between output current and output voltage for constant input current. for C~~B~~E output current is I_c and output voltage is V_{CE} while input current is I_B.



Active Region- for given β and I_B, I_c is dependent on I_{CBO} which is more dependent on V_{CE} than the case in CB. so graph of active region has some slope showing change in I_C on changing in V_{CE}

$$I_C = \beta I_B + (\beta+1) I_{CBO}$$

Saturation region- When the transistor is switched from active region to saturation region a large change in collector current for very small change in collector voltage.

cutoff region- When both junction are reverse biased a very small collector current is obtained which is close to horizontal axis.

In CE configuration $I_c = \beta I_B + (\beta+1) I_{CBO}$.

(Q2) Define α and β with respect to BJT and derive the relationship between them. A transistor having $\alpha = 0.975$ and reverse saturation current $I_{CBO} = 10\mu A$ is operated in CE Mode. If the base current is $250\mu A$. Calculate I_E and I_C.

Sol: **α :-** It is the ratio of output current (I_C) to the input current (I_E) $\alpha = \frac{I_C}{I_E}$ since $I_E > I_C$ so value of α is less than 1. Value of α ranges from 0.90 to 0.99. no current available in CB configuration.

β :- It is the ratio of output current (I_C) to the input current (I_B). $\beta = \frac{I_C}{I_B}$ value of $I_B << I_C$ so $\beta >> 1$ and current is available in CE configuration. Value of β varies from 20 to 500.

γ :- It is the ratio of O/P current (I_E) to the Input current (I_B) $\gamma = \frac{I_E}{I_B}$ since value of $I_B << I_E$ so $\gamma >> 1$ therefore current gain available in CC configuration.

$\alpha = 0.975$ $I_B = 250\mu A$ $I_{CO} = I_{CEO} = 10\mu A$

Numericals:-

$$\boxed{\beta = \frac{\alpha}{1-\alpha}} = \frac{0.975}{1-0.975}$$

$$= \frac{0.975}{0.025} = 39 \qquad \boxed{\beta = 39}$$

Now for CE:- $I_C = \beta I_B + I_{CEO}$

$$I_C = 39 \times 250 \times 10^{-6} + 10 \times 10^{-6}$$

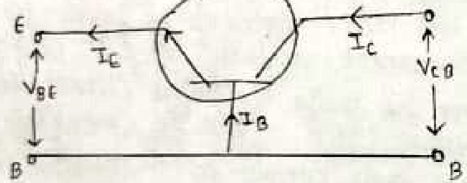
$$I_C = 9.76 mA$$

$$I_E = I_C + I_B$$

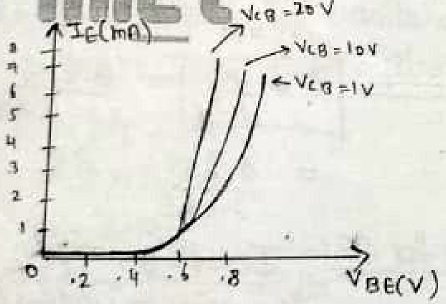
$$I_E = 9.76 + 0.25 \qquad \boxed{I_E = 10.01 mA}$$

Ⓠ3 Draw the input and output characteristics of Common base (CB) configuration. Also Write an expression For output current.

Ans



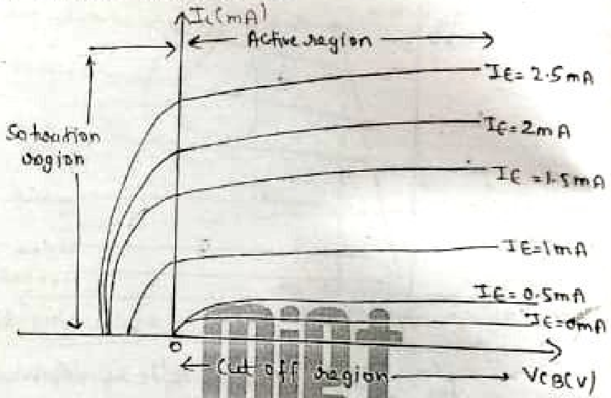
Input characteristics- It is the graph between input current and input voltage for a constant output voltage. In CB Configuration input current is I_E and input voltage is V_{BE} While output Voltage is V_{CB}.



Important point-

- → Input characteristics is identical to the V-I characteristics of forward biased diode.
- → As V_{CB} increases I_E increases slightly due to early effect

Output characteristics- It is the graph between output and output voltage for constant input current common Output current is I_C and output Voltage is V_{C} While input current is I_E.



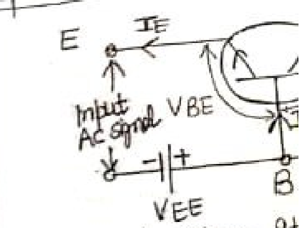
Active region- for given α and I_E, I_C is dependent on I_{CBO} which is slightly depand on V_{CB}. So graph active region is almost constant.

Saturation region- When the transistor is switched from active to saturation region, a large change in electron current for very small Value of forward bias Voltag at Collector to base junction is obtained in negative

Cut-off region- When both the junction are reverse bia a very small collector current is obtained

In CB configuration $I_C = \alpha I_E + I_{CBO}$.

xpression For Outpu



DC current gain:- It the Input current lue of α is less than o no current gain i Expression for o/p curr

then I

for CB $I_C = I_{CB}$

(Reverse Leakage C emitter is open

Q4) what is B can be defin

Ans Base Width

Forward bias profile is DE Layer formed non uniform. At towards the small. On ctuleen output current

ent Common Base

ltage is V_{CB}

$E = 2.5mA$

$E = 2mA$

$I_E = 1.5mA$

$E = 1mA$

$2.5mA$

$I_E = 0mA$

→

$B(V)$

endent only

o graph of

d from

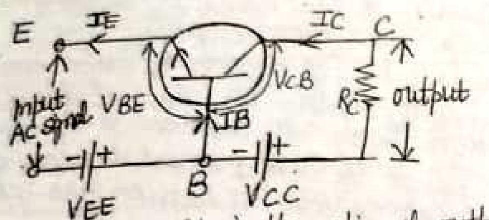
ection

Voltage

gative direct

biased

Expression for Output current:-



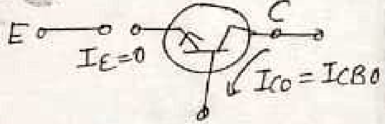
① **Dc current gain:-** It is the ratio of output current (I_C) to the Input current (I_E). $\boxed{\alpha = \frac{I_C}{I_E}}$ since $I_E > I_C$ so value of α is less than 1. Value of α ranges from ·90 to ·99 so no current gain is available in CB configuration.

⑪ **Expression for o/p current:-** $I_C = I_{ec} + I_{CO}$ but $I_{ec} = \alpha I_E$

then $I_C = \alpha I_E + I_{CO} \rightarrow$ Collector current when emitter is open.

for CB $I_C = I_{CBO}$

(Reverse Leakage current b/w collector and base while emitter is open i.e $I_E = 0$

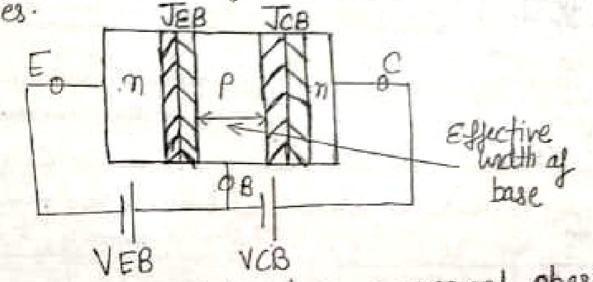


Q.4) What is Base Width Modulation? How a transistor can be defined as a current operated device?

Ans **Base Width Modulation:-** In active region JEB is forward bias and JCB is reverse bias. Also doping profile is $D_E > D_C > D_B$. So width of depletion layer formed on E-B Junction and C-B Junction is non uniform. At both junction major width of depletion is towards the base. So effective width of base is very small. On increasing V_{CB} effective width of base

base region further reduces. this effect is called base width modulation or early effect.

On increasing V_{CE} I_E and I_C increases but I_B decreases (due to reduction in base width, possibility of recombination in this region reduces. thus α, β, γ increases.



transistor can be defined as a current operated device:-

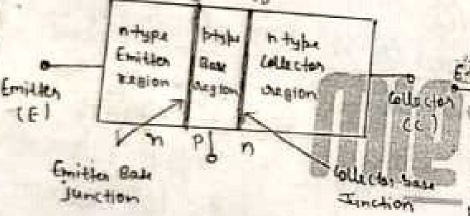
BJT is called current controlled device. because output is controlled by input current. In BJT the base current controls the current flow from emitter to collector.

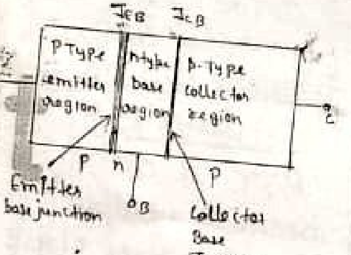
Q.5

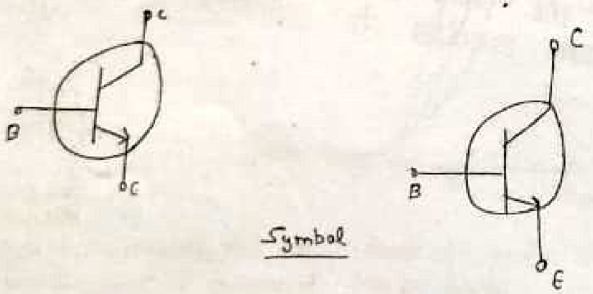
(Q.5) Discuss the construction, doping profile and physical appearance of emitter base and collector of transistor.

Ans- **Construction of transistor-**

BJT Consist of a layer of n type material sandwitched between two p-type materials or one p-type material is sandwiched between two n-type materials.







Symbol

Emitter:- It is the highest doping region in the trans supplies (emits) carries to the base. It supplie to the base in npn and holes in pnp.

Base:- It is the middle part of transistor is called, b very thin and lightly doped. So most of the c coming from emitter passes to collector.

Collector:- Collector collects the carries which are comi the base. Doping of collector is heavier than b less than emitter.

Area profile :- $C > E > B$

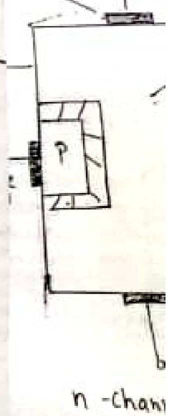
doping profile :- $E > C > B$

Why JFET is
Explain th

JFET. Dra
N/P channel

Construction

both side o
two p-n ju
nnected b
are drain a
nic contact



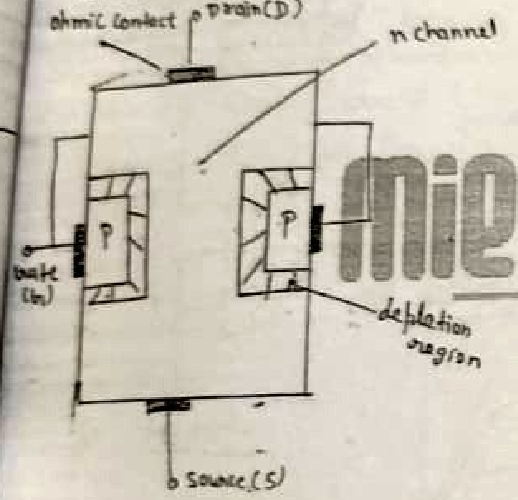
n -Chan

Operation:-

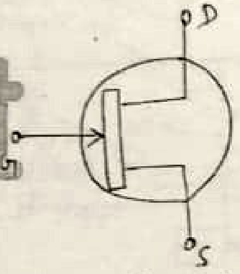
- When V
from sou
layer a
If V_{PS} i
layer just
Cond

Q6:- Why JFET is called Voltage Controlled device? Draw its structure & Explain the construction and working of N channel JFET. Draw the drain characteristics/output characteristic of N/P channel JFET indicate different regions and its significance?

Ans:- **Construction-** A n channel JFET have n type base on both side of base two heavily doped p regions are formed. so two p-n junction are formed which are internally connected by a gate terminal and other two terminals are drain and source.



n-Channel JFET



Symbol

operation:- (i) V_{DS} = positive (>0) and $V_{GS}=0$

- When V_{DS} is increased more and more electrons move from source to drain. So current increases and depletion layer also increases. So, channel becomes narrower.
- If V_{DS} is further increased a condition comes when depletion layer just touches each other. This condition is called pinch-off condition.

- The value of V_{DS} which establish this condition is called pinch-off voltage (V_P). After pinch off current becomes constant.

(ii) V_{DS} = +ve (>0) and V_{GS} = -ve (<0)

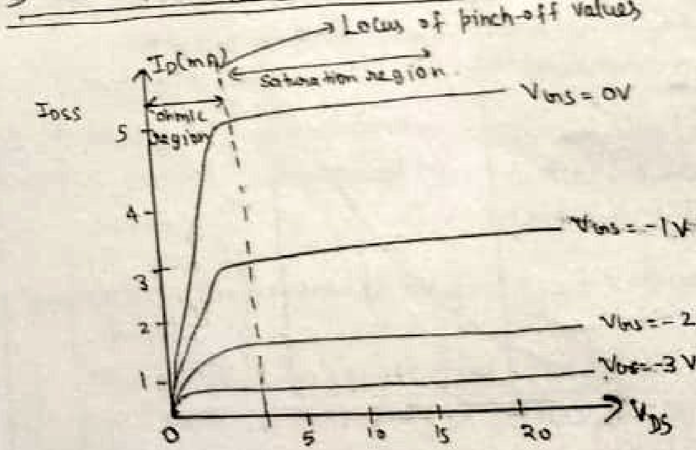
- As V_{GS} is increased pinch off condition comes earlier and pinch-off voltage decreases in parabolic manner.
- At V_{GS} = V_P, current I_D will be zero.

JFET Characteristics-

JFET has two types of characteristics

i) Drain or output characteristics
ii) Transfer characteristics

i) **Drain or Output characteristics-**



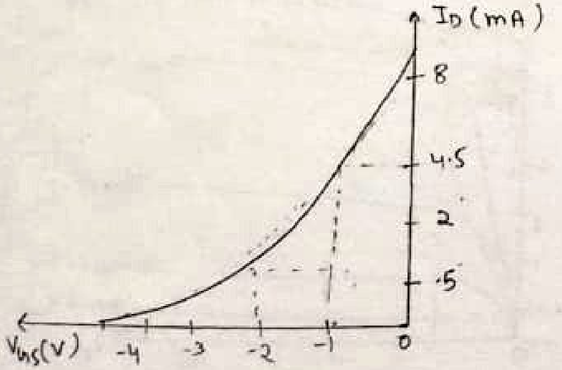
- **ohmic region**– The current I_D increases linearly with V_{DS} in ohmic region the slope of graph is dependent on V_{GS}. So FET can be used as Voltage controlled resistance.

Saturation region or Active region–

→ After pinch-off condition the drain current (I_{DSS}) and this region is called saturation region.
In this region JFET works as amplifier.

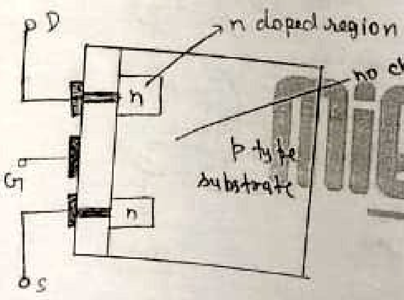
Transfer characteristics– It is the graph between drain current (I_D) and gate to source Voltage (V_{GS}) while drain to source voltage (V_{DS}) should be constant. I_D & V_{GS} are related by schokley eqn.

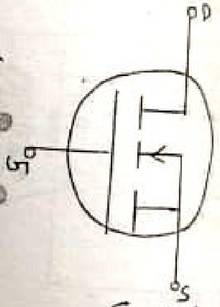
$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$



Q8- **Describe the construction working of N/P enha… MOSFET. Draw drain & Transfer characteristi…**

Ans– **Construction**:– N channel enhancement M… p type substrate. In p type substrate two n… are formed. A thin layer of SiO_2 is deposited… and source are connected with the help of metal… contact. There is no channel between two n…





Symbol

operation:–

(i) V_{DS} = +ve (>0) and V_{GS} = 0

- If V_{DS} is increased then no current will f… because there is no channel, i.e I_D=0

(ii) V_{DS} = +ve (>0) and V_{GS} = +ve (>0)

- If positive gate voltage is applied at g… then electron in p type move towards the gate and h… move away from the gate.

Till 2V no channel i… channel is formed.

This 2V is called th… V_{GS} is further increa… increases. This is ca…

characteristics– It has tw…

1) **Drain or Output ch…** between drain curren… Voltage (V_{DS}) at c…

N/P
of enchancement
acteristics.

nt MOSFET.
two n regions
sited. Drain
metallic
n regions.

PD

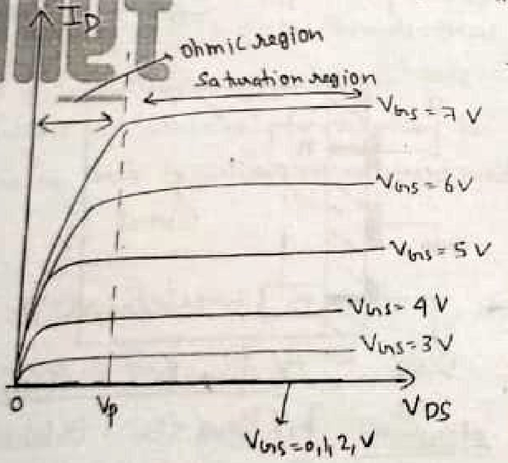
flow

gak
holes

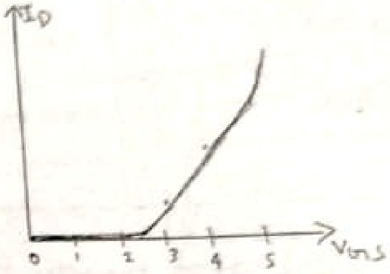
- Till 2V no channel is formed. But after 2V channel is formed.
- This 2V is called threshold Voltage (V_T). If V_{GS} is further increased then I_D continously increases. This is called enhancement MOSFET.

Characteristics- It has two types of characteristics.

(i) **Drain or output characteristics-** It is the curve between drain current (I_D) and drain to source voltage (V_{DS}) at constant gate to source voltage (V_{GS}).



(ii) **Transfer characteristics :-**



It is the curve between drain current (I_D) and gate to source voltage (V_{GS}) at constant drain to source voltage.

7 ⓠⓠ List the difference between JFET & BJT. Define Pinch off voltages & transconductance (gm) ?

Ans-

	JFET	BJT
1.	It is unipolar device. i.e. operation depends only on majority carries.	It is bipolar device i.e. operation depends on majority and minority carrier.
2.	Voltage Controlled device i.e. output is controlled by voltage.	current Controlled device. i.e. output is Controlled by Current
3.	Input impedance is very high	Input impedance is very low.
4	Temperature independent due to absence of minority Carrier	Temperature dependent due to presence of minority Carrier.

5.	Power consumption is low.	Power consumption is high.
6	more cost	less cost
7	Less noisy	More noisy

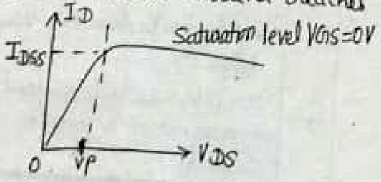
Transconductance (gm) - It is the ratio of change in drain current (ΔI_D) and change in gate to source voltage (ΔV_{GS}) at constant drain to source voltage (V_{DS})

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \Big| V_{DS} = \text{Constant}$$

$$= \frac{dI_D}{dV_{DS}}$$

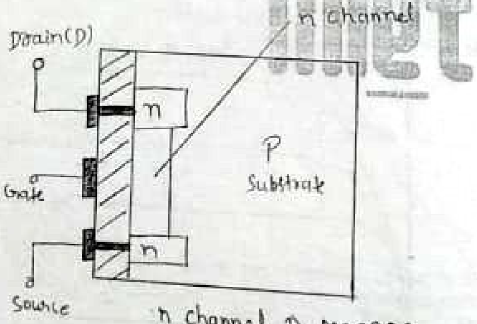
Unit of gm is Siemen.

Pinchoff voltage - (V_P) - The pinchoff voltage is the value of V_{DS} when drain current reaches saturation value, I_{DSS}

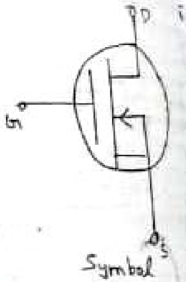


Q9 - Explain the construction and working of de → N/P type MOSFET. Also draw its drain and transfe characteristics.

Ans - Construction - n channel depletion type MOSFE p type base (substrate). Then two n regions are A thin layer of SiO_2 is deposited. Drain and source connected with metalic contact. A n channel is fo between two n regions. Gate is insulated from n ch by SiO_2. So I_G is zero. It is also called insul gate field effect transistor (IGFET)



n channel D MOSFET



Symbol

Operation - (i) $V_{GS} = 0$, $V_{DS} = +ve$

- When V_{DS} is increases more and more electron move from source to drain. so current increase a condition come when current become constant

This condition is C of V_{DS} which establi pinch-off voltage becomes constant.

ii) V_{DS} = +ve (>

- If V_{GS} is in move towards th So, recombinatio so, pinch-off voltage decrease depletion mode

iii) V_{DS} = +ve (>0

- If positive V in p type sub
- So number o current V_{GS}

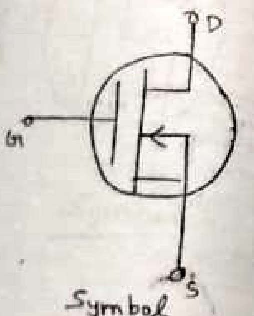
Characteris

It has tw

i) Drain or between source Vol source V

ion and working of depletion → N/P ch
its drain and transfer

depletion type MOSFET has
Then two n regions are form
nited. Drain and source are
act A n channel is formed
is insulated from n channel
I is also called insulated
nFET)



Symbol

d more electrons
current Increases
come constant.

- This condition is called pinch-off condition. The value of V_{DS} which established this condition is called pinch-off Voltage (V_P). After pinchoff current becomes constant.

(ii) $V_{DS} = +ve\ (>0)$, $V_{GS} = -ve\ (<0)$:-

- If V_{GS} is increased then holes in p type substrate move towards the channel.
- So, recombination process occurs in channel.
- so, pinch-off condition comes earlier and pinch-off voltage decreases in parabolic manner. This is called depletion mode

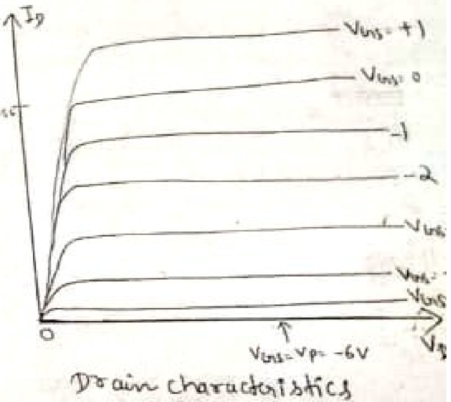
(iii) $V_{DS} = +ve\ (>0)$ and $V_{GS} = +ve\ (>0)$:-

- If positive Voltage is applied at gate then electrons in p type substrate move towards the channel.
- So number of electrons in channel increases. So current V_{GS} increases. This is called enhancement mode.

Characteristics-

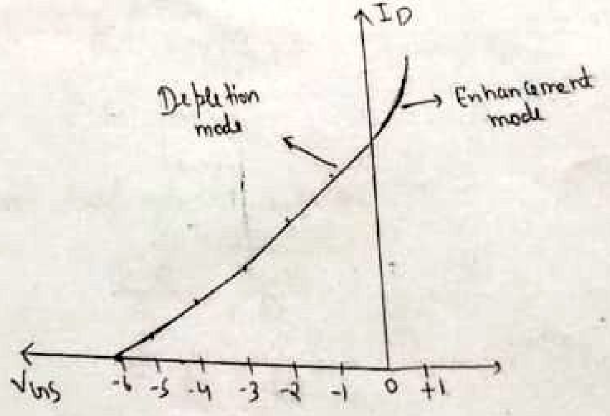
It has two types of characteristics.

i) Drain or output characteristics. It is the curve between drain current (I_D) and drain to source Voltage (V_{DS}) at constant gate to source Voltage. (V_{GS})



Drain characteristics

ii) Transfer characteristics- It is the curve between drain current (I_D) and gate to source Voltage at constant drain to source voltage (V_{DS}).



UNIT-3

---

* UNIT-3RD *

(Q.1) what is an operational amplifier ? Draw and expla diagram. Write the characteristic of an ideal op

Ans OP-amp is a direct coupled high gain amp can be used to amplify ac as well as dc signal. g used for mathematical operation like addition, subtra Integration, differentiation etc & hence named as o amplifier. Block diagram of Operational Amplif

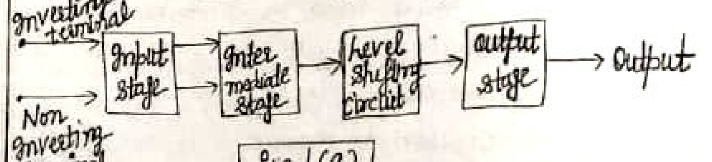


fig 1(a)

Input stage:- the Input stage is the dual input balance o (DIBO) differential amplifier. Its function is to amplify difference between two input signals. It provides hi differential gain, high input Impedence.

Intermediate Stage:- The Overall gain requirement of an is very high. Intermediate stage is used to provide required additional gain. It consist of another d amplifier with dual input and unbalanced (Single end

Level Shifting circuit:- As the OP-amp amplifies dc also, the small dc voltage Level of previous stage amplified and applied as the input to the next stage distortion in the final output. So Level Shifting Circu used to bring down the Dc Level to ground potential

Output stage:- It is the final stage which is usually consist of a push pull complementry amplifier - the stage decreases the Impedance and increases the cu supplying capability of the op-amp.

---

aracteristic of an ideal

aracteristic:-

pen loop gain should be

$Ad(A_{VOL}) = \infty$

Input resistance should be

$R_i = \infty$

slew rate should be infini

$SR = \infty$

Input offset voltage shoul

$V_{IO} = 0$

Input offset current

$I_{IO} = 0$

(5) what do you mean OP-amp for the in mplifier has differen

CMRR:- It is mode signal (NOISE) fferential mode ga

$\boxed{CMRR = \frac{Ad}{AC}}$

For ideal op-amp CMRR in dB.

Fe

C

Numerical:- CM

Vd

Vc

CMRR=

Vout = A

Vout = 4

Vout =

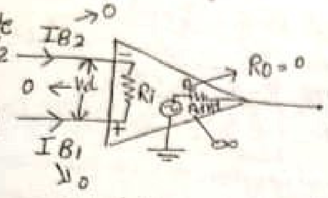
characteristic of an ideal operational amplifier:-

characteristic:-

(I) open loop gain should be infinite
$Ad(A_{VOL}) = \infty$

(II) Input resistance should be infinite
$R_i = \infty$

(III) slew rate should be infinite
$SR = \infty$



(IV) Input offset voltage should be zero.
$V_{IO} = 0$

(V) Input bias current should be zero
$I_B = 0$

(VI) Input offset current should be zero
$I_{IO} = 0$

(VII) CMRR should be infinite
$CMRR = \infty$

(Q.5) what do you mean by CMRR? determine the output voltage of an op-amp for the input voltage of $V_1 = 150\mu V$ and $V_2 = 140\mu V$. the amplifier has differential gain $Ad = 4000$ and $CMRR = 100$.

Ans **CMRR:-** It is the ability of a op-amp to reject the common mode signal (Noise). Successfully CMRR is defined as the ratio differential mode gain (Ad) and common mode gain (AC)

$$\boxed{CMRR = \frac{Ad}{AC}}$$

for noise (ideal op-amp) $AC = 0$ So $CMRR = \infty$

for ideal op-amp CMRR is ∞ but for Practical op-amp It is 90dB.

CMRR in dB.

$$\boxed{CMRR = 20\log_{10}\frac{Ad}{AC}}$$

Numerical:- $CMRR = 100$ where $V_1 = 150\mu V$ $V_2 = 140\mu V$

$Vd = V_1 - V_2$ then $Vd = 150 - 140 = 10\mu V$

$Vc = \frac{V_1 + V_2}{2}$ $Vc = \frac{150+140}{2} = \frac{290}{2} = 145\mu V$

$$\boxed{CMRR = \frac{Ad}{AC}}$$

where $Ad = 4000$ then $100 = \frac{4000}{AC}$

$$\boxed{AC = \frac{4000}{100} = 40}$$

$$\boxed{V_{out} = Ad\,Vd + AC\,VC}$$

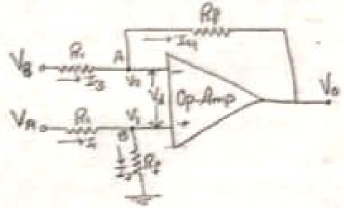
$V_{out} = 4000 \times 10 \times 10^{-6} + 40 \times 145 \times 10^{-6}$

$V_{out} = 4 \times 10^{-2} + 580 \times 10^{-5} = (4 + 0.58) \times 10^{-2} = 4.58 \times 10^{-2}$

$$\boxed{V_{out} = 45.8\,mV}$$

Q8/. Draw and explain difference & Summing amplifier.

Ans/. Difference or Subtractor amplifier:- A circuit that amplifies the difference between two input signal is called difference amplifier or Subtractor amplifier.



Expression for Output Voltage:-

Apply KCL at Node B

$I_1 = I_2$

$\frac{V_A - V_1}{R_1} = \frac{V_1 - 0}{R_f}$

$\frac{V_A}{R_1} - \frac{V_1}{R_1} = \frac{V_1}{R_f}$

$\frac{V_A}{R_1} = \frac{V_1}{R_1} + \frac{V_1}{R_f}$

$V_A = \cancel{R_1}.V_1\left(\frac{R_f + R_1}{\cancel{R_1}.R_f}\right) \Rightarrow \boxed{V_A = \left(\frac{R_1 + R_f}{R_f}\right).V_1} \Rightarrow \boxed{V_1 = \left(\frac{R_f}{R_1 + R_f}\right).V_A}$ —①

From the concept of Virtual ground

$V_d = 0$

$V_1 - V_2 = 0$

$\therefore V_1 = V_2$

But $V_1 = \left(\frac{R_f}{R_1 + R_f}\right).V_A$ [by using eqⁿ①]

So, $\boxed{V_2 = \left(\frac{R_f}{R_1 + R_f}\right).V_A}$ —②

Now, Apply KCL at node A

$I_3 = I_4$

$\frac{V_B - V_2}{R_1} = \frac{V_2 - V_o}{R_f}$

$\frac{V_B}{R_1} - \frac{V_2}{R_1} = \frac{V_2}{R_f} - \frac{V_o}{R_f}$

$\frac{V_o}{R_f} = V_2\left(\frac{1}{R_1} + \frac{1}{R_f}\right) - \frac{V_B}{R_1}$

$$V_0 = R_f.\left(\frac{R_f+R_1}{R_1.R_f}\right).V_2 - \frac{R_f}{R_1}.V_B$$

$$V_0 = \left(\frac{R_1+R_f}{R_1}\right).\left(\frac{R_f}{R_1+R_f}\right).V_A - \frac{R_f}{R_1}.V_B \quad \text{[by using eq}^n \text{ ②]}$$

$$V_0 = \frac{R_f V_A}{R_1} - \frac{R_f}{R_1}V_B \Rightarrow \boxed{V_0 = \frac{R_f}{R_1}(V_A - V_B)}$$

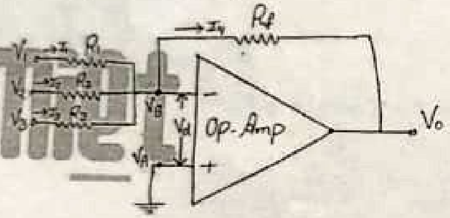
So, Circuit works as a difference or subtractor amplifier.

If $R_1 = R_f$, $\therefore \boxed{V_0 = V_A - V_B}$

So, Circuit works as a difference or Subtractor.

Summing Amplifier:- Summing amplifier is an Op-Amp circuit which Can accept two more inputs and produces output as the sum of these inputs.

Expression for o/p voltage:-



Here, $V_A = 0$ —— ①

From Concept of virtual ground

$V_d = 0$

$V_A - V_B = 0$

$\therefore V_A = V_B$

But $V_A = 0$, $\therefore \boxed{V_B = 0}$

Apply KCL at node A

$$I_1 + I_2 + I_3 = I_4$$

$$\frac{V_1 - V_B}{R_1} + \frac{V_2 - V_B}{R_2} + \frac{V_3 - V_B}{R_3} = \frac{V_B - V_0}{R_f}$$

But $V_B = 0$, $\therefore \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_0}{R_f}$

$$\boxed{V_0 = -\left[\frac{R_f}{R_1}.V_1 + \frac{R_f}{R_2}.V_2 + \frac{R_f}{R_3}.V_3\right]}$$

Case 1st:- If $R_1 = R_2 = R_3 = R$

then, $\boxed{V_0 = -\frac{R_f}{R_1}[V_1 + V_2 + V_3]}$ So, Circuit works as Summing amplifier.

Case 2nd:- If $R_1 = R_2 = R_3 = R_f$

then $\boxed{V_0 = -[V_1 + V_2 + V_3]}$ So, Circuit works as a

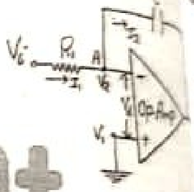
Case 3rd:- If $R_1 = R_2 = R_3 = 3R_f$

then $\boxed{V_0 = -\left[\frac{V_1 + V_2 + V_3}{3}\right]}$ So, Circuit works as an

Q4/. Draw the circuit of an integrator and differentiator and explain its working.

Ans/. **Integrator**:- A circuit that performs the integration signal is called integrator Circuit.

Expression for output voltage:-



Here, $V_1 = 0$ —— ①

from Concept of Virtual ground

$V_d = 0$

$V_1 - V_2 = 0$

$\therefore V_1 = V_2$

But $V_1 = 0$

So $\boxed{V_2 = 0}$

Apply KCL at node A

$$I_1 = I_2$$

$$\frac{V_i - V_2}{R_1} = C\frac{dV_c}{dt}$$

$$\frac{V_i - V_2}{R_1} = C\frac{d(V_2 - V_0)}{dt}$$

But $V_2 = 0$, $\frac{V_i}{R_1} = C\frac{d(-V_0)}{dt}$

$$\frac{V_i}{R_1} = -C\frac{dV_0}{dt}$$

$$dV_0 = -\frac{1}{R_1C}V_i\,dt$$

---

taking integration on both

$$\int dV_0 = \int -\frac{1}{R_1C}V_i\,dt$$

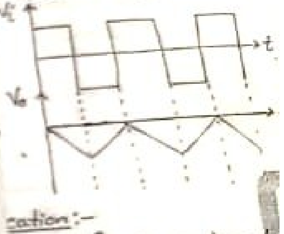
$$\boxed{V_0 = -\frac{1}{R_1C}\int_0^t V_i\,dt}$$

$$V_0 \propto \int_0^t V_i\,dt$$

output voltage is directly

hence circuit is called

t wave for Square input



cation:-

used for generating t

is used in digital to a

is used as low pass f

entiator:- A Circuit

ut signal is called

ssion for output voltag

Here $V_1 = 0$ —— ①

Concept of virtual

$V_d = 0$

$V_1 - V_2 = 0$

$\therefore V_1 = V_2$

but $V_1 = 0$

So, $\boxed{V_2 = 0}$

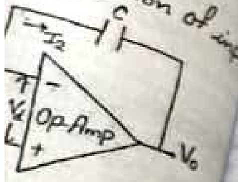
pply KCL at Node

t works as a summer

rks as an average c

l differentiator w

integration of inp



---

now taking integration on both side

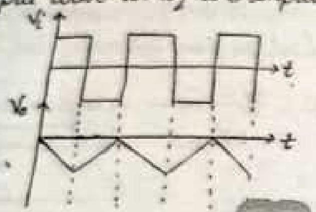
$$\int dV_0 = \int -\frac{1}{RC} V_i\, dt$$

$$\boxed{V_0 = -\frac{1}{RC}\int_0^t V_i\, dt}$$

$$V_0 \propto \int_0^t V_i\, dt$$

nce output voltage is directly proportional to the integration of input ignal, hence circuit is called integrator circuit.

utput wave for square input:-

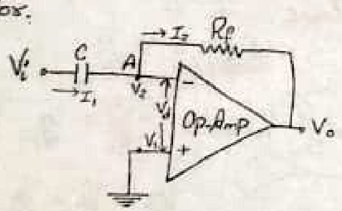


Application:-

- It is used for generating triangular wave.
- It is used in digital to analog converter circuit.
- It is used as low pass filter.

Differentiator:- A circuit that performs the mathematical differentiation of input signal is called differentiator.

Expression for output voltage:-



Here $V_1 = 0$ —①

from concept of virtual ground

$V_d = 0$

$V_1 - V_2 = 0$

$\therefore V_1 = V_2$

but $V_1 = 0$

So, $\boxed{V_2 = 0}$

Apply KCL at Node A, $I_1 = I_2$

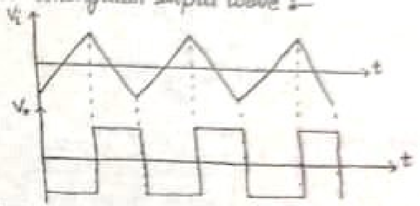
$$C\frac{dV_i}{dt} = \frac{V_2 - V_0}{R_f}$$

$$C\frac{d(V_i - V_2)}{dt} = \frac{V_2 - V_0}{R_f}$$

But $V_2 = 0$, $C\frac{dV_i}{dt} = -\frac{V_0}{R_f} \Rightarrow \boxed{V_0 = -R_f C\frac{dV_i}{dt}} \Rightarrow \boxed{V_0 \propto \frac{dV_i}{dt}}$

Since output voltage is directly proportional to the differentiation of input signal, so, circuit is called differentiator circuit.

Output for triangular input wave:-

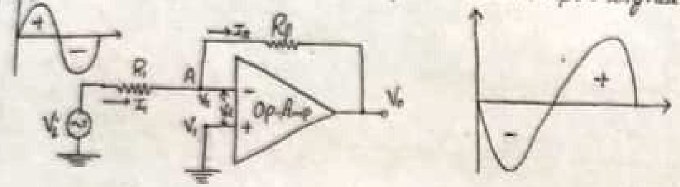


Application:-

- It is used to generate square wave.
- It is also used in analog to digital converter circuit.
- It is used as high pass filter.

Q4/ Explain the working of non inverting & inverting amplifier. Also derive the expression for output voltage.

Ans/ Inverting Amplifier :- An Op-Amp circuit that produce an amplified output signal that is 180° out of phase with input signal.



Expression for O/P Voltage :-

Here $V_1 = 0$ —— ①

From Concept of Virtual ground

$V_d = 0$

$V_1 - V_2 = 0$

$\therefore V_1 = V_2$

But $V_1 = 0$ [by eq^n ①]

So, $\boxed{V_2 = 0}$ — ②

By Applying KCL at Node A

we have, $I_1 = I_2$

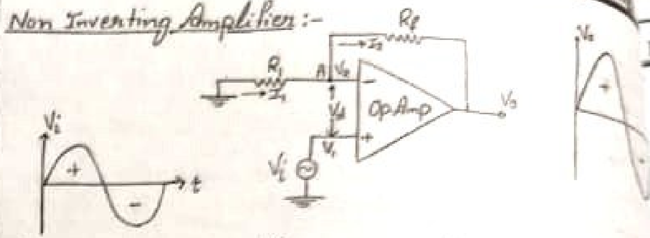
$$\frac{V_i - V_2}{R_1} = \frac{V_2 - V_o}{R_f}$$

But $V_2 = 0$, $\therefore \frac{V_i}{R_1} = -\frac{V_o}{R_f}$

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{R_f}{R_1}}$$

- The negative sign denotes a 180° phase difference b/w I/p & O/P.
- Gain can be set to any value by manipulating the value of R_f & R_1.

Non Inverting Amplifier :-



A non-inverting amplifier is an Op-Amp circuit design to voltage gain. The input is directly applied to non-inv

Expression for output voltage :-

Here $V_1 = V_i$ —— ①

From concept of Virtual ground

$V_d = 0$

$V_1 - V_2 = 0$

$\therefore V_1 = V_2$

But $V_1 = V_i$ [by eq^n ①]

So, $\boxed{V_2 = V_i}$ —— ②

By applying KCL at Node A

we have, $I_1 = I_2$

$$\frac{0 - V_2}{R_1} = \frac{V_2 - V_o}{R_f}$$

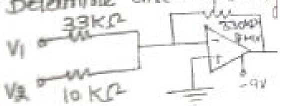
But $V_2 = V_i$, $\therefore -\frac{V_i}{R_1} = \frac{V_i}{R_f} - \frac{V_o}{R_f}$

$$\frac{V_o}{R_f} = \frac{V_i}{R_f} + \frac{V_i}{R_1}$$

$$\frac{V_o}{V_i} = \frac{R_f}{R_f} + \frac{R_f}{R_1} \Rightarrow \boxed{A_v = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}}$$

- The positive sign denotes that I/P and O/P are in same phase
- Gain can be set to any value by manipulating the value of

Determine the output o



this is the inverting

$V_o = -\left[\frac{R_F}{R_1} V_1\right.$

where $R_F = 330$ k

$V_1 = V_2 = 0.15$ V

$V_o = -\left[\frac{33}{33}\right.$

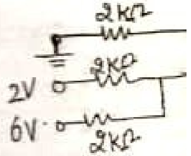
$= -\left[\frac{49}{3}\right.$

$= -[1.5$

$\boxed{V_o = -6}$

explain the Conce

the Output voltage



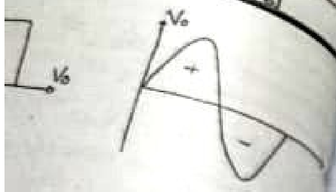
Concept of

for an ideal op-amp

$V_o =$

$V_d = \frac{V_o}{A_d}$ $V_d =$

So $V_1 - V_2 = 0$



circuit design to provide
d to non-inverting te

e phase.
e of Rf & R1.

(Q.6) Determine the output of following circuit Given V1 = V2 = 0.15V

Sol: this is the Inverting Scaling Amplifier.

$$V_0 = -\left[\frac{R_F}{R_1}V_1 + \frac{R_F}{R_2}V_2\right]$$

where $R_F = 330\,k\Omega$ $R_1 = 33\,k\Omega$ $R_2 = 10\,k\Omega$

$V_1 = V_2 = 0.15V$

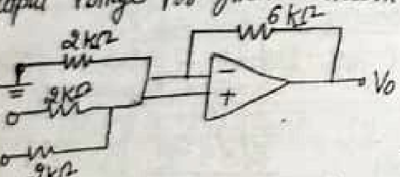
$$V_0 = -\left[\frac{330}{33}\times 0.15 + \frac{330}{10}\times 0.15\right]$$

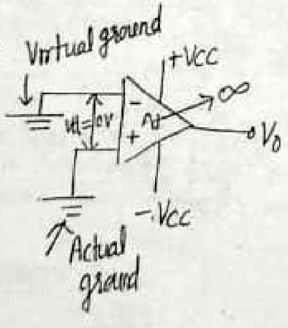
$$= -\left[\frac{49.5}{33} + \frac{49.5}{10}\right]$$

$$= -[1.5 + 4.95]$$

$$\boxed{V_0 = -6.45V}$$

(Q.7) explain the Concept of virtual ground in OP-AMP. Determine the Output voltage for given Network.





Ans Concept of Virtual ground :-

For an ideal op-amp $A_d = \infty$

$V_0 = A_d V_d$

$V_d = \frac{V_0}{A_d}$ $V_d = \frac{V_0}{\infty} = 0$

So $V_1 - V_2 = 0$ then $\boxed{V_1 = V_2}$

If one terminal of op-amp is connected to ground then other terminal will also be at ground. this is called concept of virtual ground. concept of virtual ground is used to determine closed loop voltage gain and output voltage.

Numerical :- this is non inverting Adder. Hence we have

$V_0 = A_{VF} \times V_1$

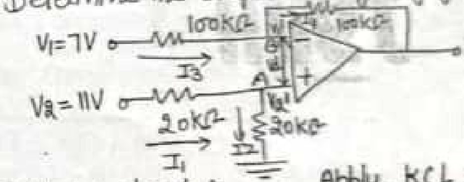
$$V_0 = \left[1 + \frac{R_F}{R_1}\right] \times \left(\frac{V_a + V_b}{2}\right)$$

$$V_0 = \left[1 + \frac{6}{2}\right] \times \left[\frac{2+6}{2}\right]$$

$$= [1+3] \times [4] = 16 \text{ volts}$$

$$\boxed{V_0 = 16 \text{ volts}}$$

(Q.8) Determine the output voltage of following circuit.



Sol: Apply KCL at Node A

$\underline{I_1 = I_2}$

$$\frac{V_2 - V_2'}{R_1} = \frac{V_2'}{R_2}$$

$$\frac{11 - V_2'}{20} = \frac{V_2'}{20}$$

$20(11 - V_2') = 20V_2'$

$220 - 20V_2' = 20V_2'$

$40V_2' = 220$

$\boxed{V_2' = 5.5\,k\Omega}$

Apply KCL at Node B

$\underline{I_3 = I_4}$

$$\frac{V_1 - V_1'}{R_3} = \frac{V_1' - V_0}{R_4}$$

where due to virtual ground concept

$\underline{V_1' = V_2'}$

then $\frac{7 - 5.5}{100} = \frac{5.5 - V_0}{100}$

$1.5 = 5.5 - V_0$

$+V_0 = -5.5 + 1.5 = +4$

$\boxed{V_0 = 4 \text{ Volts}}$ Ans

UNIT-4

UNIT :- 4th

Q1. Convert the following :- (1) $(2CCD)_{16} = (\ )_8 = (\ )_5$

Sol: In Hexadecimal → $(\ )_2$ → 0010 1100 1100 1101

$(\ )_8$ → 0 2 6 3 1 5 ⇒ (02

$(026315)_8 \longrightarrow (\ )_5$

Step I :- $(026315)_8 \longrightarrow (\ )_{10}$

0 2 6 3 1 5

→ $8^5\ 8^4\ 8^3\ 8^2\ 8^1\ 8^0$

→ $0\times8^5 + 2\times8^4 + 6\times8^3 + 3\times8^2 + 1\times8^1 + 5\times8^0$

→ $(11469)_{10}$

Step II :- $(11469)_{10} \rightarrow ($

5 | 11469 - Remainder

5 | 2293 - 4 ← LSB

5 | 458 - 3

5 | 91 - 3

5 | 18 - 1

3 - 3

↑ MSB

= (331

Ans

Q1(2) Convert $(784)_9 = (\ )_{10} = (\ )_4$

Sol:- Step I :- $(784)_9 = (\ )_{10}$

7 8 4

$9^2\ 9^1\ 9^0$

→ $7\times9^2 + 8\times9^1 + 4\times9^0$

→ 567 + 72 + 4

→ $(643)_{10}$

Step II :- $(643)_{10} = (\ )_4$

4 | 643 - Remainder

4 | 160 - 3 ← LSB

4 | 40 - 0

4 | 10 - 0

2 - 2

↑ MSB

= (22003

Ans

Q1(3) Convert the following $(637)_9 = (?)_5$

Sol:- Step I :- $(637)_9 \rightarrow (\ )_{10}$

6 3 7

$9^2\ 9^1\ 9^0$

→ $6\times9^2 + 3\times9^1 + 7\times9^0$

→ 486 + 27 + 7

→ $(520)_{10}$

Step II :- $(520)_{10} = (\ )_5$

5 | 520 - Remainder

5 | 104 - 0 ← LSB

5 | 20 - 4

4 - 0

↑ MSB

$= (4040)_5$ Ans

Q2(i) Determine base of the foll

Suppose $(345)_{10} = (531)_x$

345 = 531

$10^2\ 10^1\ 10^0$ = $x^2\ x^1\ x^0$

→ $3\times10^2 + 4\times10^1 + 5\times10^0 = 5x^2$

→ 300 + 40 + 5 $= 5x^2$

→ 345 = $5x^2 + 3x^1 +$

$5x^2 + 3x - 344 = 0$

suppose we take x = 8

$5(8)^2 + 3\times(8) - 344$

$5\times64 + 24 - 344 = 0$

344 - 344 = 0

0 = 0

Q2(ii) $(2374)_{16} = (9076)_x$

Sol: 2374 = 907 6

$16^3\ 16^2\ 16^1\ 16^0$ $x^3\ x^2\ x^1\ x$

$2\times16^3 + 3\times16^2 + 7\times16^1 + 4\times16^0 = 9x^3$

8192 + 768 + 112 + 4 $= 9x^3 +$

9076 $= 9x^3 + 7x + 6$

$9x^3 + 7x - 9070 = 0$

$9(10)^3 + 7\times(10) - 907$

9000 + 70 - 9070 =

then $\boxed{(2374)_{1}}$

Q2(iii) Subtract using 10's com

Sol:- Suppose A = 9754 B =

find A - B = ? using 10's

First find 10's complement of B =

Note:- 10's complement of a no is 1

its 9's complement no

9's complement of 364 is :-

then add 1 =

Now add 9636 with A

= 9754
  9636

19390

carry

$CD)_{16} = (\ )_8 = (\ )_5$

$10\,1100\,1100\,1101$

$6\ \ 3\ \ 1\ \ 5 \Rightarrow (026315)$

pII :- $(11469)_{10} \rightarrow (\ )_8$

11469	– Remainder
2293	– 14 ← LSB
458	– 13
91	– 13
	– 11
	– 13

$= (331334$

Ans

$43)_{10} = (\ )_4$

ainder

– LSB

$= (22003)_4$

Ans

$)_5$

$_{10} = (\ )_5$

der

SB

$0)_5$ Ans

Q.2(I) Determine base of the following :- (I) $(345)_{10} = (531)_X$

Sol: Suppose $(345)_{10} = (531)_X$

$$\overset{\uparrow}{3}\overset{\uparrow}{4}\overset{\uparrow}{5} = \overset{\uparrow}{5}\overset{\uparrow}{3}\overset{\uparrow}{1}$$

$$10^2\,10^1\,10^0 = x^2\,x^1\,x^0$$

$\rightarrow 3\times10^2 + 4\times10^1 + 5\times10^0 = 5X^2 + 3X^1 + 1X^0$

$\rightarrow 300 + 40 + 5 = 5X^2 + 3X^1 + 1$

$\rightarrow 345 = 5X^2 + 3X^1 + 1$

$5X^2 + 3X - 344 = 0$ ——— Ⓐ

Suppose we take $X = 8$ then put into eq Ⓐ.

$5(8)^2 + 3\times(8) - 344 = 0$ then Value of $X = 8$

$5\times64 + 24 - 344 = 0$

$344 - 344 = 0$ Now

$0 = 0$

$$\boxed{(345)_{10} = (531)_8}$$

Ans

Q.2(II) $(2374)16 = (9076)X$

Sol: $\underset{16^3 16^2 16^1 16^0}{2374} = \underset{x^3 x^2 x^1 x^0}{9076}$

$2\times16^3 + 3\times16^2 + 7\times16^1 + 4\times16^0 = 9X^3 + 0X^2 + 7X^1 + 6X^0$

$8192 + 768 + 112 + 4 = 9X^3 + 7X + 6$

$9076 = 9X^3 + 7X + 6$

$9X^3 + 7X - 9070 = 0$ — Ⓐ Assume $X = 10$ put $X = 10$ in eq Ⓐ

$9(10)^3 + 7\times(10) - 9070 = 0$

$9000 + 70 - 9070 = 0 \Rightarrow 9070 - 9070 = 0$

$0 = 0$

then $\boxed{(2374)_{16} = (9076)_{10}}$ Ans

Q.2(III) Subtract using 10's complement : $(9754)_{10} - (364)_{10}$

Sol:- Suppose $A = 9754$ $B = 364$

find $A - B = ?$ using 10's complement

First find 10's complement of $B = 364$

Note:- 10's complement of a no is 1 added to its 9's complement no.

$$\begin{array}{r} 9999 \\ -\ 364 \\ \hline 9635 \end{array}$$

9's complement of 364 is :-

then add 1 $= \begin{array}{r} 9635 \\ +1 \\ \hline 9636 \end{array}$

Now add 9636 with A

$$= \begin{array}{r} 9754 \\ 9636 \\ \hline \boxed{1}9390 \end{array}$$

carry

the Left Most Bit of result is called carry & it is ignored So answer is $= (9390)_{10}$

Verification :- $\begin{array}{r} 9754 \\ -\ 364 \\ \hline 9390 \end{array}$

then $\boxed{(9754)_{10} - (364)_{10} = (9390)_{10}}$ Ans

Q.2(I) subtract using 1's complement : $(10111)_2 - (110011)_2$

Sol:- We have $A = 10111$ and $B = 110011$

Step(i) First we obtain 1's complement of B as 001100

Step(ii) then we add A and 1's complement of B

$$\begin{array}{rr} A = & 10111 \\ \text{1's complement of } B = & +001100 \\ \hline & \boxed{0}100011 \end{array}$$

Zero final carry → $\boxed{0}100011$ ← final answer

Here It may be Noted that as the final carry is 0. then answer is –Ve and is in its 1's complement form.

Step(iii) then we invert the final answer

Since the final answer is in 1's complement form we have to invert it to obtain the true answer.

thus $100011 \xrightarrow{\text{Invert}} 011100 = (28)_{10}$

Hence the answer is $\boxed{-(28)_{10}}$ Ans

Q.3 State De Morgan's Law. Simplify the Boolean Function using Boolean Algebra theorems. ① $A'B'C' + A'BC' + AB'C' + ABC'$

Sol: De Morgans Law:- there are two deMorgan's Law.

① Two separate term NORed together is the same as two term inverted (complement) and AND'ed i.e $\boxed{(A+B)' = A' \cdot B'}$

② two separate term Nanded together is same as the two term inverted (complement) and OR'ed i.e $\boxed{(A \cdot B)' = A' + B'}$

① $A'B'C' + A'BC' + AB'C' + ABC'$

Sol: $= A'C'(\underline{B'+B}) + AC'(\underline{B'+B})$

$= A'C'(1) + AC'(1)$ $\because B' + B = 1$

$= C'(\underline{A'+A})$ $\because A' + A = 1$

$= C'$ Ans

② $(A+B+C)(A+B'+C')(A+B+C')(A+B'+C)$

$= (AA + AB' + AC' + BA + BB' + BC' + AC + B'C + C'C)$

$\cdot (\underset{A}{\underline{AB}} + AB' + AC + AB + B'B + BC + AC' + B'C' + C'C)$

$= (A + AB' + AC' + AB + BC' + AC + B'C) \cdot (A + AB + AC + AB + BC + AC' + B'C)$

$= (A(\underset{1}{\underline{1+B'}}) + AC' + AB + BC' + AC + B'C) \cdot (A(\underset{1}{\underline{1+B'}}) + AC + AB + BC + AC' + B'C')$

$= (A(\underset{1}{\underline{1+C'}}) + AB + BC' + AC + B'C)(A(\underset{1}{\underline{1+C}}) + AB + BC + AC' + B'C')$

$= (A(\underset{1}{\underline{1+B}}) + BC' + AC + B'C)(A(\underset{1}{\underline{1+B}}) + BC + AC' + B'C')$

$= (A(\underline{1+C}) + BC' + B'C)(A(\underline{1+C'}) + BC + B'C')$

$= (A + BC' + B'C)(A + BC + B'C')$

$= (AA + ABC + AB'C' + ABC' + \underline{BCBC'}$
$+ \underset{0}{\underline{BCB'C}} + AB'C + \underset{0}{\underline{BCB'C}} + \underset{0}{\underline{B'CB'C'}})$

$= (A + ABC + AB'C' + ABC' + AB'C)$

$= (A + ABC + AB'C + AB'C' + ABC')$

$= (A + AC(\underset{1}{\underline{B+B'}}) + AC'(\underset{1}{\underline{B'+B}}))$

$= (A + AC + AC')$

$= (A + A(\underset{1}{\underline{C+C'}}))$

$= (\underline{A + A})$

$= A$ Ans

continue →

Q4(i) what are Universal gates ? why are they called so?

Sol: A Universal gate is a gate which can implement any boolean function without need of any other gate. the Nand and NOR are called Universal gate. this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families.

NAND Gate:- This is NOT-AND Gate. the output of Nand gate is high (1). if any of the input is low. truth table:-

Input A	Input B	output $Y=\overline{A\cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate:-

this is NOT-OR gate. the output of NOR gate is low if any one of the Input is high.

truth table:-

Input A	Input B	output $Y=\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Q4-ii) Draw the logic diagram of EX-OR gate using Universal gate (NAND and NOR)?

Sol: EX-OR using NAND Gate :-

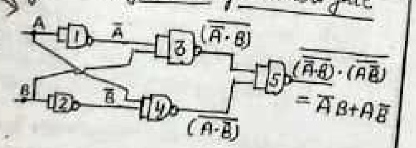
Method Ist :- EX-OR:-

$Y = \bar{A}B + A\bar{B}$

$Y = \overline{\overline{\bar{A}B + A\bar{B}}}$ [∵ $\bar{\bar{A}} = A$]

$= \overline{\underbrace{(\overline{\bar{A}B})\cdot(\overline{A\bar{B}})}_{5}}$

=



Method-2nd :- EX-OR :-

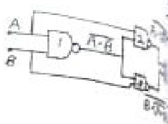
$Y = \bar{A}B + A\bar{B} + A\cdot\bar{A} + B\cdot\bar{B}$ [∵ $A\cdot\bar{A}=0$ & $B\cdot\bar{B}=0$]

$= A(\bar{A}+\bar{B}) + B(\bar{A}+\bar{B})$

$= A(\overline{A\cdot B}) + B(\overline{A\cdot B})$ [∵ $\overline{A\cdot B} = \bar{A}+\bar{B}$]

$= \overline{\overline{A(\overline{A\cdot B}) + B(\overline{A\cdot B})}}$ [∵ $\bar{\bar{A}} = A$]

$= \overline{\underbrace{\underbrace{\overline{A\cdot\underbrace{(\overline{A\cdot B})}_{1}}}_{2}\cdot\underbrace{\overline{B\cdot\underbrace{(\overline{A\cdot B})}_{1}}}_{3}}_{4}}$ [∵ $\overline{A+B} = \bar{A}\cdot\bar{B}$]



EX-OR Gate Using NOR Gate :-

Method- Ist :- EX-OR :-

$Y = \bar{A}B + A\bar{B}$

$= \overline{\overline{\bar{A}B + A\bar{B}}}$ [∵ $\bar{\bar{A}} = A$]

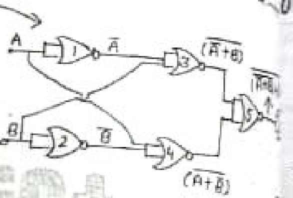
$= \overline{(\overline{\bar{A}\cdot B})\cdot(\overline{A\cdot\bar{B}})}$ [∵ $\overline{A+B} = \bar{A}\cdot\bar{B}$]

$= \overline{(\bar{\bar{A}}+\bar{B})\cdot(\bar{A}+\bar{\bar{B}})}$ [∵ $\overline{A\cdot B} = \bar{A}+\bar{B}$]

$= \overline{(A+\bar{B})\cdot(\bar{A}+B)}$ [∵ $\bar{\bar{A}} = A$]

$= \overline{\overline{(A+\bar{B})}+\overline{(\bar{A}+B)}}$ [∵ $\overline{A\cdot B} = \bar{A}+\bar{B}$]

$= \underbrace{\underbrace{\overline{\overline{\underbrace{\overline{(A+\underbrace{\bar{B}}_{2})}}_{3}+\underbrace{\overline{(\underbrace{\bar{A}}_{1}+B)}}_{4}}}}_{5}}_{6}$



Method 2ND:- EX-OR:-

$Y = \bar{A}B + A\bar{B} + A\cdot\bar{A} + B\cdot\bar{B}$

$= \bar{A}(A+B) + \bar{B}(A+B)$ [∵ $A\cdot\bar{A}=0$ & $B\bar{B}=0$]

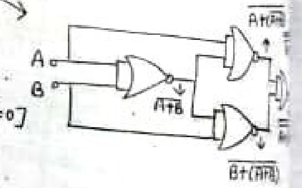
$= \overline{\overline{\bar{A}\cdot(A+B) + \bar{B}(A+B)}}$ [∵ $\bar{\bar{A}} = A$]

$= \overline{[\overline{\bar{A}\cdot(A+B)}]\cdot[\overline{\bar{B}\cdot(A+B)}]}$ [∵ $\overline{A+B} = \bar{A}\cdot\bar{B}$]

$= \overline{[\bar{\bar{A}}+(\overline{A+B})]\cdot[\bar{\bar{B}}+(\overline{A+B})]}$ [∵ $\overline{A\cdot B} = \bar{A}+\bar{B}$]

$= \overline{[A+(\overline{A+B})]}+\overline{[B+(\overline{A+B})]}$ [∵ $\overline{A\cdot B} = \bar{A}+\bar{B}$]

$= \underbrace{\overline{\overline{\underbrace{\overline{\underbrace{[A+(\overline{A+B})]}_{2}}+\overline{\underbrace{[B+(\overline{A+B})]}_{3}}}_{4}}}}_{5}$



) what are MAXTERM and MI

$Y(A,B,C,D) = (A+B+$

MAX TERM:- Each term

alled max term. It is repr

maxterm uncomplemented Va

l complemented Variable is

NTERM:- Each term in Stan

esented by m. minterm is

able is represented by 1 (i

0 (i.e $\bar{A}=0$) } $\bar{A}=0$, $A=1$ }

$Y = (A+B+C)\cdot(A+D)$

$= (A+B+C+D\bar{D})\cdot($

$= (A+B+C+D)\cdot(A+B+C$

$(A+\bar{B}+\bar{C}+D)$

$= (A+B+C+D)\cdot(A+B+C+\bar{D})\cdot$

$\cdot(A+B+\bar{C}+D)\cdot(A$

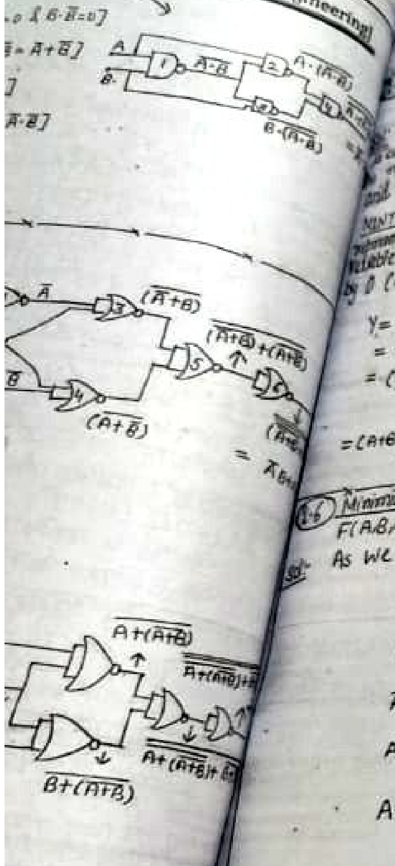
) Minimize the following

$F(A,B,C,D) = AB'C' + A'$

As we know this is

AB \ CD	$\bar{C}\bar{D}$ 00
$\bar{A}\bar{B}$ 00	
$\bar{A}B$ 01	
AB 11	
$A\bar{B}$ 10	

$\boxed{F(A,B,C,D) = A\bar{B}}$



(Q.5) what are MAXTERM and MINTERM ? Convert the following into POS Format:
$Y(A,B,C,D) = (A+B+C)\cdot(A+D)$

MAX TERM:- Each term in Standard or canonical POS (Product of Sum) is called max term. It is represented by m. maxterm is opposite of minterm. maxterm uncomplemented variable is represented by 0 (i.e A=0) and Complemented variable is represented by 1. (i.e $\bar{A}=1$) $\left\{\begin{matrix}\bar{A}=1\\A=0\end{matrix}\right\}$

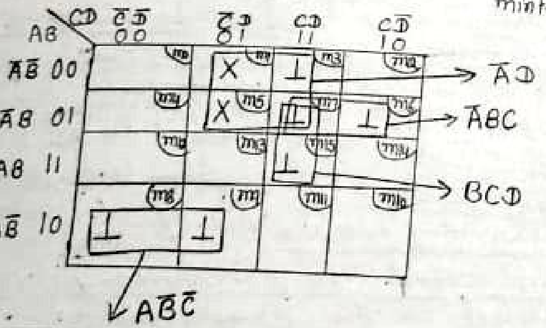
MINTERM:- Each term in Standard or canonical SOP is called minterm. It is represented by m. minterm is opposite of max term. In minterm uncomplemented variable is represented by 1 (i.e A=1) and Complemented variable is represented by 0 (i.e $\bar{A}=0$) $\left\{\begin{matrix}\bar{A}=0\\A=1\end{matrix}\right\}$

$$Y = (A+B+C)\cdot(A+D)$$
$$= (A+B+C+D\bar{D})\cdot(A+B\bar{B}+C\cdot\bar{C}+D)$$
$$= \underline{(A+B+C+D)}\cdot(A+B+C+\bar{D})\cdot\underline{(A+B+C+D)}\cdot(A+\bar{B}+C+D)\cdot(A+B+\bar{C}+D)\cdot(A+\bar{B}+\bar{C}+D)$$
$[\because A\cdot A = A]$
$$= (A+B+C+D)\cdot(A+B+C+\bar{D})\cdot(A+\bar{B}+C+D)\cdot(A+B+\bar{C}+D)\cdot(A+\bar{B}+\bar{C}+D)$$
$[\because (A+B+C+D)\cdot(A+B+C+D)=(A+B+C+D)]$

Ans

(Q.6) Minimize the following using K-MAP technique:-
$F(A,B,C,D) = AB'C' + A'BC + A'B'CD + ABCD + d(1,5)$

Sol:- As we know this is SOP Condition so $\bar{A}=0$ & $A=1$ & these are minterms.

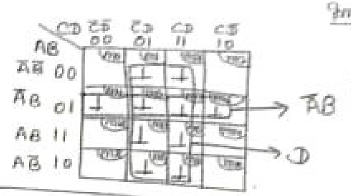


$$\boxed{F(A,B,C,D) = A\bar{B}\bar{C} + BCD + \bar{A}BC + \bar{A}D}$$

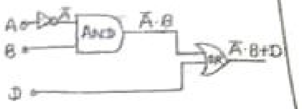
Ans

(Q.7) Simplify the following function using K-map.
$F(A,B,C,D) = \Sigma(1,3,4,5,6,7,9,11,13,15)$ Also Implement the simplified function using basic gates only

Sol: this is SOP condition. So these are minterms. Here $\bar{A}=0$ & $A=1$



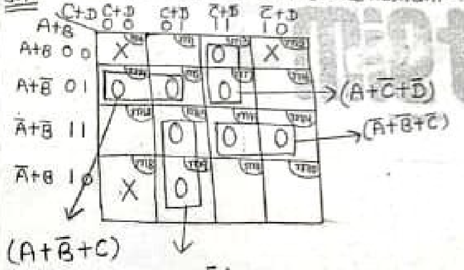
Implementation Using Basic Gates



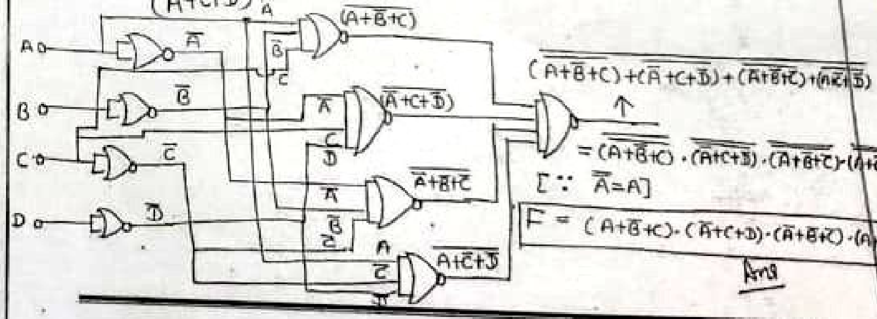
$$\boxed{F(A,B,C,D) = \bar{A}\cdot B + D}$$

(Q.8) Minimize using K-map and realize using NOR gates only.
$F(A,B,C,D) = \Pi M(3,4,5,7,9,13,14,15)\cdot d(0,2,8)$

Sol:- this is POS condition. So these are maxterm. then $A=0$ & $\bar{A}=1$



$$\bar{F} = (A+\bar{B}+C)\cdot(\bar{A}+C+\bar{D})\cdot(\bar{A}+\bar{B}+\bar{C})\cdot(A+\bar{C}+\bar{D})$$
$$F = \bar{\bar{F}}$$



$$\overline{\overline{(A+\bar{B}+C)}+\overline{(\bar{A}+C+\bar{D})}+\overline{(\bar{A}+\bar{B}+\bar{C})}+\overline{(A+\bar{C}+\bar{D})}}$$
$$= \overline{\overline{(A+\bar{B}+C)}}\cdot\overline{\overline{(\bar{A}+C+\bar{D})}}\cdot\overline{\overline{(\bar{A}+\bar{B}+\bar{C})}}\cdot\overline{\overline{(A+\bar{C}+\bar{D})}}$$
$[\because \bar{\bar{A}}=A]$

$$\boxed{F = (A+\bar{B}+C)\cdot(\bar{A}+C+D)\cdot(\bar{A}+\bar{B}+\bar{C})\cdot(A+\bar{C}+\bar{D})}$$

Ans

UNIT-5

UNIT-5

Q1) Draw and explain the block diagr Communication system. (Or) Explain the elements communication system with the help of block diagram

Ans → Communication is the transfer of info from point A to point B using electricity or m Communication can be divided into three parts i) Transmitter (ii) Channel (iii) Receiver.

(i) **Transmitter:** The Transmitter section co

(A) **Information source** : It is used to generat ~~msg~~ Message signal which may be in the form audio, video or data.

(B) **TRANSducer** :- It is a device which conv One form of energy into other. Here it conv raw message signal into electrical signal.

(C) **Modulator** - Here low frequency message signal is superimposed on high frequency carrier signal so that it can cover long distance.

(D) **Amplifier** — This block is used to ~~eh~~ enhance strength of the signal before transmission.

(E) **Transmitting Antenna** : It is used to convert electrical signal into electromagnetic wave, whic can travel in the atmosphere.

(ii) **Channel**:- The EM waves radiated from transmitting antenna travels through a path or Medium to reach receiver. This path or medium is called channel.

There are two

Wired Channel :

i.e optical fib

Wireless Chann

i) **Noise** : It i

with the transm

There are tw

) natural nois

) man made no

are automob

iii) **Receiver**

A) Receiving

received en

the electrica

B) **Amplifier**

has suffered

so an ampli

C) **Demodulat**

from t

(D) **Transdu**

Convert

form to o

There are two types of Channel.

Wired Channel : Here the medium is physical i.e optical fibre, coaxial Cable etc.

Wireless Channel : Here Medium is air.

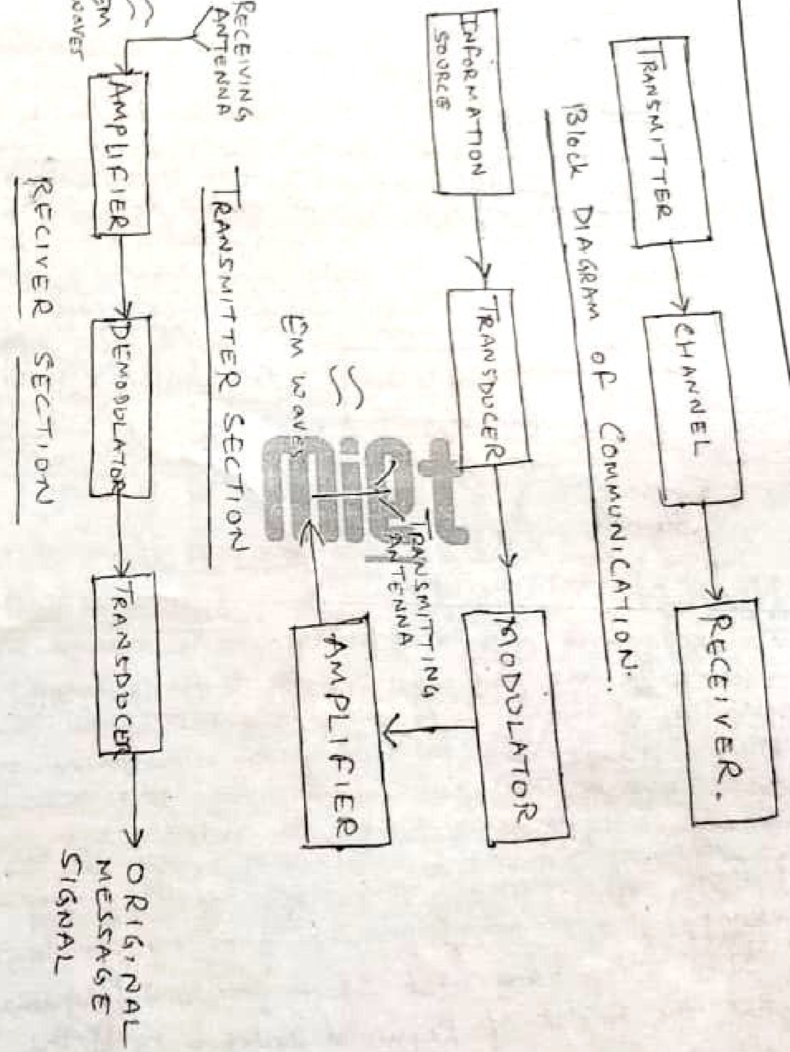
Noise : It is unwanted signal which will mix with the transmitted signal when it is in channel. There are two types of noise.

natural noise : The source of natural noise is radiation from sun and stars

man made noise : The source of man made noise are automobiles, motors etc.

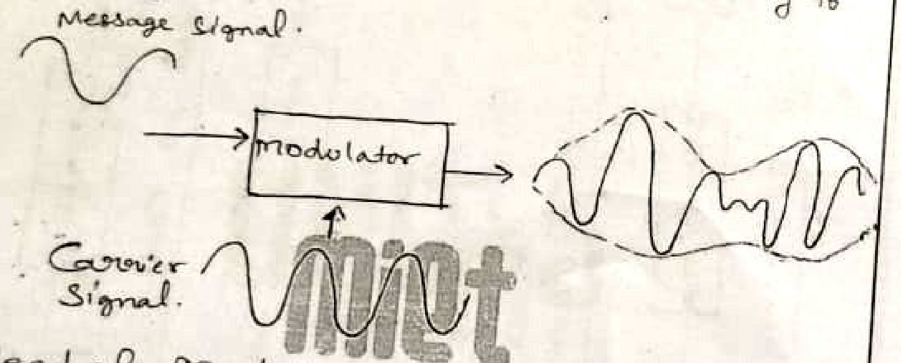
i) **Receiver** : This section Consist of.

- **Receiving Antenna** → It is used to convert received em waves from the channel into the electrical signal.
- **Amplifier** : The signal received at the receiver has suffered various types of losses in the atmosphere. so an amplifier is needed to increase its strength.
- **Demodulator** : It is used to separate carrier from the message signal
- **Transducer** : Finally this circuit is used to Convert received message signal in the electrical form to original form (it may be text, audio, data).



Q2 (I) What is Modulation? why modulation is required in Communication System?

Ans MODULATION :→ It is a process in which low frequency message signal is superimposed on the high frequency Carrier wave. In this Process one of the parameters of the Carrier varies according to the message Signal.



Need of Modulation.

(a) Interference or mixing Problem :→ As message signals are generally low frequency Signals there is large Probability of mixing with other signals of the same frequency range also present in the atmosphere. so low frequency message Signals are sent through high frequency Carrier wave to aviod such problems.

(b) Height of Antenna:- Practical height of transmitting or receiving antenna = $\frac{\lambda}{4}$, where λ is the wavelength of the signal being used. If we use low frequency Signal, the height of Required antenna is of the order of kilometers.

part see from booklet

Power dissipation.

Q2-II The antenna current of an AM transmitter is 8 when only the carrier is sent, but it increases 8.93A. when the carrier is modulated by a single sine wave. find Percentage modulation. Determine antenna current when the Percent of modulation changes to 0.8.

Sol:- We know that

$$I_t = I_C\sqrt{1+\frac{m^2}{2}} \quad \text{—} Ⓐ$$

where transmitting current of Antenna $I_t = 8.93A$

carrier current $I_C = 8A$

put the values of It & Ic in eq Ⓐ then we get

$$I_t = I_C\sqrt{1+\frac{m^2}{2}}$$

$$\frac{I_t}{I_C} = \sqrt{1+\frac{m^2}{2}}$$

taking square both side then $\left(\frac{I_t}{I_c}\right)^2 = \left(\sqrt{1+\frac{m^2}{2}}\right)^2$

$$\frac{I_t^2}{I_c^2} = 1+\frac{m^2}{2} \Rightarrow \frac{(8.93)^2}{(8)2} = 1+\frac{m^2}{2}$$

$$\frac{79.7449}{64} = 1+\frac{m^2}{2}$$

$$1.2460 = 1+\frac{m^2}{2}$$

$$\frac{m^2}{2} = 0.2460$$

$$m^2 = 0.4920$$

$$m = \sqrt{0.4920}$$

$$\boxed{m = 0.7014}$$

% Modulation $= m \times 100$
$= 0.7014 \times 100$
$= 70.14\%$

$$\boxed{\% \; m = 70.14}$$

nics Engineering]
mitter is 8A
t increase
by a single
Determine
dulation
8.93A
get.
$\left(\frac{m^2}{2}\right)^2$

(1) Q3 What is amplitude Modulation? Derive its expression and also draw its frequency spectrum. Explain with the help of proper waveform. Derive the expression for the total power radiated by modulated signal. Also calculate modulation efficiency.

Amplitude Modulation:- In amplitude Modulation, the amplitude of the Carrier Signal is modulated according to the instantaneous amplitude of the message signal. In this process frequency and phase of the Carrier remains Constant.

Expression of Amplitude Modulated (AM) Signal.

$m(t) = V_m \cos(2\pi f_m t)$

$c(t) = V_c \cos(2\pi f_c t)$

$$\boxed{m = \frac{V_M}{V_C}}$$

m is modulation Index

$$S_{Am}(t) = [V_c + m(t)] \cos 2\pi f_c t.$$

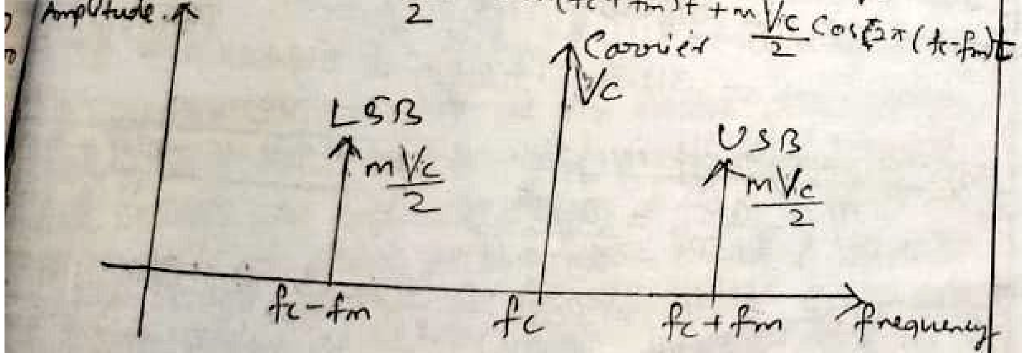
$$= [V_c + V_m \cos(2\pi f_m t)] \cos 2\pi f_c t.$$

$$\Rightarrow V_c \cos 2\pi f_c t + V_m \cos 2\pi f_m t \cos 2\pi f_c t$$

$$\Rightarrow V_c \cos 2\pi f_c t + \frac{V_m}{2}[\cos 2\pi(f_c + f_m)t + \cos 2\pi(f_c - f_m)t]$$

$$\Rightarrow V_c \cos 2\pi f_c t + \frac{V_m}{2}\frac{V_c}{V_c} \cos 2\pi(f_c + f_m)t + \frac{V_m}{2}\cdot\frac{V_c}{V_c}\cos 2\pi(f_c - f_m)t$$

$$\Rightarrow V_c \cos 2\pi f_c t + m\frac{V_c}{2}\cos 2\pi(f_c + f_m)t + m\frac{V_c}{2}\cos 2\pi(f_c - f_m)t$$



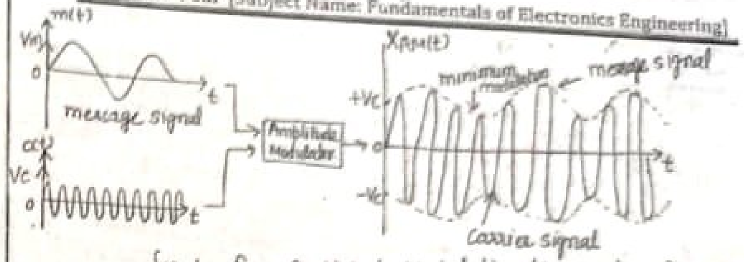


fig 1 For Amplitude Modulation / (Waveform)

expression for total power radiated by the Modulated signal & efficiency:- AM wave has three components. Unmodulated carrier, lower sideband & upper side band.

therefore $P_{Total} = P_C + P_{USB} + P_{LSB}$

$$= \frac{V^2_{Carrier}}{R} + \frac{V^2_{USB}}{R} + \frac{V^2_{LSB}}{R}$$

① **Carrier Power P_C:-**

$P_C = \frac{V_C^2}{R}$ → carrier power

∵ the average carrier power $= \frac{(V_C/\sqrt{2})^2}{R} = \frac{V_C^2}{2R}$

② **Power in side band:-** $P_{USB} = P_{LSB} = \frac{\left(\frac{mV_C}{2\sqrt{2}}\right)^2}{R} = \frac{m^2V_C^2}{8R} = \frac{m^2P_C}{4}$

③ **Total Power P_t:-** $P_t = P_C + P_{USB} + P_{LSB}$

$$P_t = P_C + \frac{m^2P_C}{4} + \frac{m^2P_C}{4} = P_C\left(1 + \frac{m^2}{2}\right)$$

④ **Transmission Efficiency:- η:-** It is the ratio of the transmitted power which contains the information (i.e sum of lower side band power and upper side band power) to the total transmitted power P_T.

$$\text{Transmission efficiency:- } \eta = \frac{P_{LSB} + P_{USB}}{P_T} = \frac{\left[\frac{m^2P_C}{4} + \frac{m^2P_C}{4}\right]}{P_C\left[1 + \frac{m^2}{2}\right]} = \frac{\frac{m^2}{2}}{1 + \frac{m^2}{2}}$$

$$\boxed{\eta = \frac{m^2}{2 + m^2}}$$

$$\% \eta = \frac{m^2}{2 + m^2} \times 100\%.$$

(83-ii) Am radio transmitter radiates 6 kw power when modulation % is 70% Determine the Carrier power.

Ans For Am signal, power relation is

$$P_t = P_c\left(1 + \frac{m^2}{2}\right)$$

Here $P_t = 6\ kw$, $m = 0.70$

so, $$P_c = \frac{P_t}{1 + \frac{m^2}{2}} = \frac{6 \times 10^3}{1 + \frac{0.49}{2}}$$

$$= 4.82\ kw$$

(84) An Audio frequency signal $5 \sin 2\pi \times 500t$ is used to amplitude Modulate a Carrier of $25 \sin 2\pi \times 10^5 t$, Calculate (i) Modulation Index (ii) Side band frequency (iii) Amplitude of each side band (iv) Bandwidth required. (V) Total Power (VI) Transmission Efficiency.

Ans Given: $m(t) = 5 \sin 2\pi \times 500t$

$c(t) = 25 \sin 2\pi \times 10^5 t$.

(i) Modulation index, $m = \frac{A_m}{A_c} = \frac{5}{25} = 0.2$ Ans

(ii) Side band frequency: $f_c + f_m$ & $f_c - f_m$

Here $f_c = 10^5\ Hz = 100\ kHz$

& $f_m = 500\ Hz = 0.5\ kHz$

so $f_c + f_m = 100 + 0.5 = 100.5\ kHz$

& $f_c - f_m = 100 - 0.5 = 99.5\ kHz$ } Ans.

(iii) Amplitude of side bands $= \frac{m \cdot A_c}{2}$ or $\frac{m \cdot}{2}$

$$= \frac{0.2 \times 25}{2}$$

$$= 2.5V$$ Ans.

(iv) Band width $= 2f_m = 2 \times 500\ Hz$

$= 1\ kHz$ Ans

(V) Total Power $P_t = P_c\left(1 + \frac{m^2}{2}\right)$

where P_c = carrier power

$P_c = \frac{V_c^2}{2R}$ where $R = 1\ \Omega$ $V_c = 25$

then $\boxed{P_c = \frac{(25)^2}{2 \times 1} = \frac{625}{2} = 312.50\ Watt}$

$$P_t = P_c\left(1 + \frac{m^2}{2}\right)$$

$$= 312.50\left(1 + \frac{(0.2)^2}{2}\right)$$

$$= 312.50\left(1 + \frac{0.04}{2}\right) = 312.50 \times 1.02$$

$$= 318.7500$$

$\boxed{P_t = 318.75\ Watt}$

(VI) transmission efficiency:-

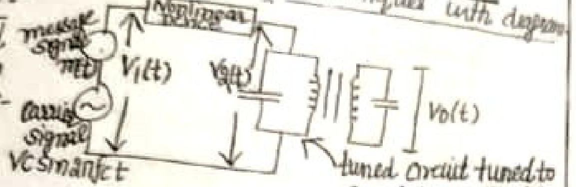
$$\eta = \frac{m^2}{2 + m^2} = \frac{(0.2)^2}{2 + (0.2)^2}$$

$$\eta = \frac{0.04}{2 + 0.04} = \frac{0/04}{2/04} = \frac{4}{204} = \frac{1}{51} = 0.0196$$

$\boxed{\%\eta = 0.0196 \times 100 = 1.96\%}$ Ans

Q.5) Describe AM modulation & Demodulation techniques with diagram

Amplitude Modulator:-



Ans: AM signal can be generated with the help of square law modulator circuit as shown:-
This circuit consist of
① a nonlinear device
② A bandpass filter
③ Carrier source and modulating signal.

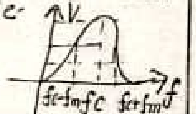
$V_1(t) = m(t) + V_c \sin 2\pi f_c t$ — ①

$V_2(t) = a V_1(t) + b V_1^2(t)$ — ②

put ① in eq ② $V_2(t) = a[m(t) + V_c \sin 2\pi f_c t] + b[m(t) + V_c \sin 2\pi f_c t]^2$

$V_2(t) = \underbrace{a\,m(t)}_{\text{message signal}} + \underbrace{a V_c \sin 2\pi f_c t}_{\text{carrier signal}} + \underbrace{b\,[m^2(t)}_{\text{squared message signal}} + \underbrace{V_c^2 \sin^2 2\pi f_c t}_{\text{squared carrier signal}} + \underbrace{2 V_c\, m(t) \sin 2\pi f_c t]}_{\text{AM wave with only sidebands}}$

In these term only 2nd & 5th term are useful. Here LC tuned circuit is used acting as bandpass filter. It frequency response.

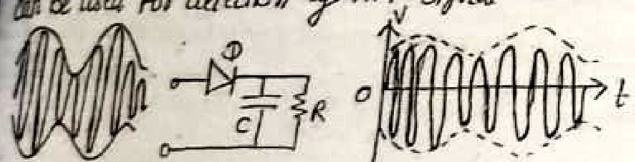


$V_o(t) = a V_c \sin 2\pi f_c t + 2 b V_c\, m(t) \sin 2\pi f_c t$

$V_o(t) = [a V_c + 2 b\, m(t)] \sin 2\pi f_c t$

square law modulator can be used to generate AM signal. BW = 2fm

Amplitude demodulator:- Linear diode detector or envelope detector can be used for detection of AM signal.



Here diode is Working as main detecting Component.

So sometimes this circuit is also called diode detector. During positive cycle of the input (modulated) signal diode conducts and capacitor charges to its peak value. During negative cycle, the diode gets reverse biased & capacitor discharge through resistor R. So the o/p voltage across capacitor is a spiky envelope of the AM wave, which is same as the message signal.

Q6.) Describe briefly Satellite Communication! Enlist the merits of satellite communication.

Answer A satellite is a smaller object that revolves around a larger object in space. For Example, Moon is a natural satellite of earth. When communication takes place between two earth stations through a satellite, then it is called as satellite communication. In this communication, E.M. waves are used as carrier signals. These signals carry the information such as voice, audio, video or any other data between ground and space and viceversa.

There are two types of satellite
i) Artifical ii) Natural

a) Artifical Satellite → Artifical satellites are specially designed and launched into space for different applications such as:- Weather monitoring, navigation, T.V, Mobile communication, planetary research etc.
Ex → INSAT, IRS, GSAT etc.

b) A natural Satellite → Natural Satellite is any celestial body in space that orbits around a large body. Earth revolves around Sun, so it is a Satellite. Similarly moon revolves around earth, so it is also a natural Satellite.

Application of satellite communication:- ① telephone, television, Digital Cinema, Radio broadcasting, Internet access, Military, Disaster management, Amateur radio.

Need of Satellite Communication :-

In communication process, transmission of signals used to occur in two different ways in earlier days. These are- ground wave propogation and sky wave propogation. But maximum distance of communication is limited to 1500km in both propogations. Satellite communication overcomes this limitation. Here communication beyond line of sight distance is possible.

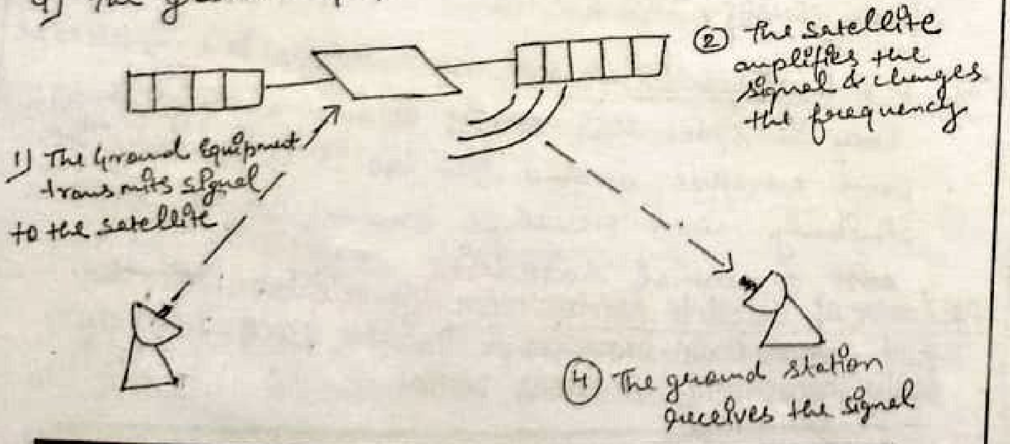
Working→ Satellite communication involves four steps:-

1] An Uplink earth station or other ground equipment transmits the desired signal to the satellite. The frequency with which the signal is transmitted is called Uplink frequency.

2] The satellite amplifies the incoming and changes the frequency.

3] The satellite transmits the signal back to Earth
The freq. of the signal is transmitted ~~is called~~
to earth is called Downlink freq.

4] The ground equipment receives the signal.



Q7(i) what is RADAR? Write down two appl
of RADAR.

Ans Radar is a detection System that uses radio waves to determine the range angle velocity of the objects. It can be used to dete aircraft, ships, spacecraft, guided missiles etc.

Elements of Radar Communication Syst

① Transmitter
② Antenna
③ Receiver
④ Power supply.

Radio wave from the transmitter, ref off the object & return to the receiver, gi information about the object's location and speed.

down two applica

that uses

range angle a

used to detec

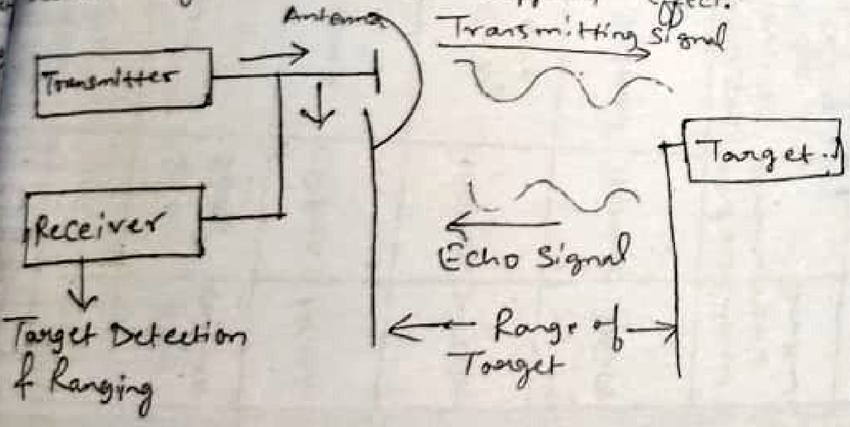
ed missiles

ation System

r, reflec

r, giving

Transmitter of radar system emits radio waves in predetermined direction. When these signals meets an object, they are usually reflected in many directions. The signals reflected back towards the Radar receiver are used for deflection purpose. The time taken by the radar signal to reach the destination & return back to the radar receiver is used for obtaining the range of the object to be detected. If the object is not fixed & moving away or towards the transmitter, there will be slight change in the frequency of received signal due to Doppler effect.



RADAR Application :- ① In Military Applications ② Air traffic Control ③ Remote sensing ④ Ground traffic Control ⑤ Space.

(Q.7(b)) Write short Notes on Wireless Communication.

Wireless Communication:- Wireless Communication is the transmission of voice and data without cable or wires. In place of a physical connection, data travels through electromagnetic signal broadcast from sending facilities to intermediate and end user devices.

the first wireless communication went on the air in the early 20th century using radiotelegraphy, which is radio communication using Morse code or other coded signal. Later as Modulation made it possible to transmit voice and music wirelessly, the medium became known as radio. Wireless transmitter use electromagnetic waves to carry voice, data, video, or signals over a communication path. where examples of Wireless devices are, cellular phone, cordless telephones, GPS, cordless computer system, Wireless LAN, Wireless Routers.

(Q.8) Explain different generations and standards in cellular communication. :-

Sol: Evolution of Mobile communication:- Mobile Wireless communication system has gone through several evolution stages in the past few decades after the introduction of first generation. Mobile network in early 1980s. Due to huge demand for more connection worldwide, mobile communication standard advanced rapidly to support more users.

1G (First Generation Mobile Network):- the first generation of mobile Network was deployed in Japan by Nippon telephone & telegraph company in 1979. the system used analog signals & it had many drawbacks due to technology limitations.

2G (Second Generation):- this generation saw the introduction of GSM (Global system for Mobile Communication) technology in the early 90's. It allowed digital voice & data to be sent across the network and allowed users to roam for First time.

2.5 G (2.5 Generation):- In the begining of 2000, an upgradation in technology introduced the packet network which provided high speed data transfer and internet and this generation is called 2.5 G. these are used in GPRS,, Packet radio, & EDGE,

3G (third Generation):- It was introduced in 2001. the major aims of third generation mobile network were to facilitate greater voice and data Capacity. these are used in video calls, chatting, conferencing, Mobile, TV, Video on demand services, navigational maps, Mobile gaming etc.

4G (Fourth Generation):- started in 2010. It is enhanced version of 3G. Network developed by IEEE. offers higher data rate and capable to handle more advanced multimedia services. LTE & LTE advanced Wireless technology are used in 4G system. Wireless transmission technology like Wimax are used in 4G system to enhance data rate and network performance.

5G (fifth Generation):- this generation is using advanced technologies to deliever ultra data fast internet and multimedia experience for customers. In order to achieve higher data rate, 5G technology will use millimeter waves and unlicensed spectrum for data transmission. complex Modulation techniques has been developed to support massive data rate.

Q.8 Write short note on evolution of Mobile Com
from 1G to 5G.

Generation Type	Year	Multiplexing	Bandwidth	Data rate	Application
1G	1980 – 1990	FDMA	30KHz	2.4 kbps	Voice (Analog)
2G	1921 – 2000	TDMA	200KHz	14.4 kbps	Voice & Digital
2.5G	2001 – 2004	TDMA CDMA	200KHz	115kbps	Voice, Sms, mms.
3G	2005 – 2010	CDMA	5 – 20 MHz	7.2 Mbps	Voice, Sms, mms + video calling
4G	2011 – 2020	OFDMA	100MHz	100Mbps	HD & UHD Streaming
5G	2021 onward.	NOMA.	1 – 2GHz	10Gbps	Enhanced Mobile Broadband